EXHIBIT 20

EXHIBIT 20

INFRINGEMENT OF U.S. PATENT NO. 6,710,406 B2

AOS AO4410 POWER MOSFET

CLAIM	AO4410 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AO4410 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AO4410-1 (datasheet); Fig. AO4410-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4410-1 (datasheet); Fig. AO4410-3 (Scanning Electron Microscopy image), item A; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending to a first depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. In the language of the claim, the predetermined depth to which the trench extends is a "first depth." (Fig. AO4410-3 (Scanning Electron Microscopy image), item B; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO4410-3 (Scanning Electron Microscopy image), item C; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AO4410-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type, and formed into the substrate to a second depth that is less than said first depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well (a second depth) is less than the predetermined depth of the trench (a first depth). (Fig. AO4410-3 (Scanning Electron Microscopy image), item D; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item D.)
a heavy body formed in said doped well extending to a third depth that is less than said second depth of said doped well, the heavy body forming an abrupt junction with the well;	The accused device has a heavy body formed in the doped well that extends to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AO4410-3 (Scanning Electron Microscopy image), item E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item E.) The junction between the doped P-type heavy body and the doped well is an abrupt junction. (Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).)
wherein, a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The location of the abrupt junction of the accused device is such that it creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench. (Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).)
2. The trenched field effect transistor of claim 1	The accused device has a doped well with a substantially flat bottom. (Fig.

CLAIM	AO4410 POWER MOSFET
wherein said doped well has a substantially flat bottom.	AO4410-3 (Scanning Electron Microscopy image), item D; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AO4410-3 (Scanning Electron Microscopy image), item B; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).)
5. The trenched field effect transistor of claim 1 wherein the heavy body comprises a heavily doped region having dopants of the second conductivity type at the abrupt junction.	The heavy body of the accused device is a heavily doped region of P-type dopants (a second conductivity type). (Fig. AO4410-3 (Scanning Electron Microscopy image), item E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item E.)
6. The trenched field effect transistor of claim 5 wherein the heavily doped region is formed by implanting dopants of the second conductivity type at approximately the third depth.	The heavy body of the accused device is formed by implanting P-type dopants (a second conductivity type) in the doped well and extending to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AO4410-3 (Scanning Electron Microscopy image), item E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item E.)
10. The trenched field effect transistor of claim 1 wherein the trench is lined with a dielectric layer and substantially filled with conductive material.	The trench of the accused device is lined with a dielectric layer and substantially filled with doped polysilicon (a conductive material). (Fig. AO4410-3 (Scanning Electron Microscopy image), items B and G; Fig. AO4410-4 (Scanning Capacitance Microscopy image), items B and G.)
11. The trenched field effect transistor of claim 10 wherein the conductive material comprises polysilicon.	The conductive material in the trench of the accused device is doped polysilicon. (Fig. AO4410-3 (Scanning Electron Microscopy image), item B; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item B.)
12. The trenched field effect transistor of claim 10 wherein the conductive material filling the trench is recessed relative to the surface of the semiconductor substrate.	The conductive polysilicon filling the trench of the accused device is recessed relative to the surface of the silicon semiconductor substrate. (Fig. AO4410-3 (Scanning Electron Microscopy image), item B; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item B.)

EXHIBIT 21

EXHIBIT 21

INFRINGEMENT OF U.S. PATENT NO. 6,710,406 B2

AOS AO4914 POWER MOSFET

CLAIM	AO4914 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AO4914 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AO4914-1 (datasheet); Fig. AO4914-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4914-1 (datasheet); Fig. AO4914-3 (Scanning Electron Microscopy image), item A; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending to a first depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. In the language of the claim, the predetermined depth to which the trench extends is a "first depth." (Fig. AO4914-3 (Scanning Electron Microscopy image), item B; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO4914-3 (Scanning Electron Microscopy image), item C; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AO4914-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type, and formed into the substrate to a second depth that is less than said first depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well (a second depth) is less than the predetermined depth of the trench (a first depth). (Fig. AO4914-3 (Scanning Electron Microscopy image), item D; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item D.)
a heavy body formed in said doped well extending to a third depth that is less than said second depth of said doped well, the heavy body forming an abrupt junction with the well;	The accused device has a heavy body formed in the doped well that extends to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AO4914-3 (Scanning Electron Microscopy image), item E; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item E.) The junction between the doped P-type heavy body and the doped well is an abrupt junction. (Fig. AO4914-5 (Secondary Ion Mass Spectroscopy data).)
wherein, a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The location of the abrupt junction of the accused device is such that it creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench. (Fig. AO4914-5 (Secondary Ion Mass Spectroscopy data).)
2. The trenched field effect transistor of claim 1	The accused device has a doped well with a substantially flat bottom. (Fig.

CLAIM	AO4914 POWER MOSFET
wherein said doped well has a substantially flat bottom.	AO4914-3 (Scanning Electron Microscopy image), item D; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AO4914-3 (Scanning Electron Microscopy image), item B; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO4914-5 (Secondary Ion Mass Spectroscopy data).)
5. The trenched field effect transistor of claim 1 wherein the heavy body comprises a heavily doped region having dopants of the second conductivity type at the abrupt junction.	The heavy body of the accused device is a heavily doped region of P-type dopants (a second conductivity type). (Fig. AO4914-3 (Scanning Electron Microscopy image), item E; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item E.)
6. The trenched field effect transistor of claim 5 wherein the heavily doped region is formed by implanting dopants of the second conductivity type at approximately the third depth.	The heavy body of the accused device is formed by implanting P-type dopants (a second conductivity type) in the doped well and extending to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AO4914-3 (Scanning Electron Microscopy image), item E; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item E.)
10. The trenched field effect transistor of claim 1 wherein the trench is lined with a dielectric layer and substantially filled with conductive material.	The trench of the accused device is lined with a dielectric layer and substantially filled with doped polysilicon (a conductive material). (Fig. AO4914-3 (Scanning Electron Microscopy image), items B and G; Fig. AO4914-4 (Scanning Capacitance Microscopy image), items B and G.)
11. The trenched field effect transistor of claim 10 wherein the conductive material comprises polysilicon.	The conductive material in the trench of the accused device is doped polysilicon. (Fig. AO4914-3 (Scanning Electron Microscopy image), item B; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item B.)
12. The trenched field effect transistor of claim 10 wherein the conductive material filling the trench is recessed relative to the surface of the semiconductor substrate.	The conductive polysilicon filling the trench of the accused device is recessed relative to the surface of the silicon semiconductor substrate. (Fig. AO4914-3 (Scanning Electron Microscopy image), item B; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item B.)

EXHIBIT 22

EXHIBIT 22

INFRINGEMENT OF U.S. PATENT NO. 6,710,406 B2

AOS AO4422 POWER MOSFET

CLAIM	AO4422 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AO4422 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AO4422-1 (datasheet); Fig. AO4422-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4422-1 (datasheet); Fig. AO4422-3 (Scanning Electron Microscopy image), item A; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending to a first depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. In the language of the claim, the predetermined depth to which the trench extends is a "first depth." (Fig. AO4422-3 (Scanning Electron Microscopy image), item B; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO4422-3 (Scanning Electron Microscopy image), item C; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AO4422-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type, and formed into the substrate to a second depth that is less than said first depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well (a second depth) is less than the predetermined depth of the trench (a first depth). (Fig. AO4422-3 (Scanning Electron Microscopy image), item D; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item D.)
a heavy body formed in said doped well extending to a third depth that is less than said second depth of said doped well, the heavy body forming an abrupt junction with the well;	The accused device has a heavy body formed in the doped well that extends to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AO4422-3 (Scanning Electron Microscopy image), item E; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item E.) The junction between the doped P-type heavy body and the doped well is an abrupt junction. (Fig. AO4422-5 (Secondary Ion Mass Spectroscopy data).)
wherein, a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The location of the abrupt junction of the accused device is such that it creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench. (Fig. AO4422-5 (Secondary Ion Mass Spectroscopy data).)
2. The trenched field effect transistor of claim 1	The accused device has a doped well with a substantially flat bottom. (Fig.

CLAIM	AO4422 POWER MOSFET
wherein said doped well has a substantially flat bottom.	AO4422-3 (Scanning Electron Microscopy image), item D; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AO4422-3 (Scanning Electron Microscopy image), item B; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO4422-5 (Secondary Ion Mass Spectroscopy data).)
5. The trenched field effect transistor of claim 1 wherein the heavy body comprises a heavily doped region having dopants of the second conductivity type at the abrupt junction.	The heavy body of the accused device is a heavily doped region of P-type dopants (a second conductivity type). (Fig. AO4422-3 (Scanning Electron Microscopy image), item E; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item E.)
6. The trenched field effect transistor of claim 5 wherein the heavily doped region is formed by implanting dopants of the second conductivity type at approximately the third depth.	The heavy body of the accused device is formed by implanting P-type dopants (a second conductivity type) in the doped well and extending to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AO4422-3 (Scanning Electron Microscopy image), item E; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item E.)
10. The trenched field effect transistor of claim 1 wherein the trench is lined with a dielectric layer and substantially filled with conductive material.	The trench of the accused device is lined with a dielectric layer and substantially filled with doped polysilicon (a conductive material). (Fig. AO4422-3 (Scanning Electron Microscopy image), items B and G; Fig. AO4422-4 (Scanning Capacitance Microscopy image), items B and G.)
11. The trenched field effect transistor of claim 10 wherein the conductive material comprises polysilicon.	The conductive material in the trench of the accused device is doped polysilicon. (Fig. AO4422-3 (Scanning Electron Microscopy image), item B; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item B.)
12. The trenched field effect transistor of claim 10 wherein the conductive material filling the trench is recessed relative to the surface of the semiconductor substrate.	The conductive polysilicon filling the trench of the accused device is recessed relative to the surface of the silicon semiconductor substrate. (Fig. AO4422-3 (Scanning Electron Microscopy image), item B; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item B.)

EXHIBIT 23

EXHIBIT 23

INFRINGEMENT OF U.S. PATENT NO. 6,710,406 B2

AOS AO4704 POWER MOSFET

CLAIM	AO4704 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AO4704 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AO4704-1 (datasheet); Fig. AO4704-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4704-1 (datasheet); Fig. AO4704-3 (Scanning Electron Microscopy image), item A; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending to a first depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. In the language of the claim, the predetermined depth to which the trench extends is a "first depth." (Fig. AO4704-3 (Scanning Electron Microscopy image), item B; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO4704-3 (Scanning Electron Microscopy image), item C; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AO4704-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type, and formed into the substrate to a second depth that is less than said first depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well (a second depth) is less than the predetermined depth of the trench (a first depth). (Fig. AO4704-3 (Scanning Electron Microscopy image), item D; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item D.)
a heavy body formed in said doped well extending to a third depth that is less than said second depth of said doped well, the heavy body forming an abrupt junction with the well;	The accused device has a heavy body formed in the doped well that extends to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AO4704-3 (Scanning Electron Microscopy image), item E; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item E.) The junction between the doped P-type heavy body and the doped well is an abrupt junction. (Fig. AO4704-5 (Secondary Ion Mass Spectroscopy data).)
wherein, a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The location of the abrupt junction of the accused device is such that it creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench. (Fig. AO4704-5 (Secondary Ion Mass Spectroscopy data).)
2. The trenched field effect transistor of claim 1	The accused device has a doped well with a substantially flat bottom. (Fig.

CLAIM	AO4704 POWER MOSFET
wherein said doped well has a substantially flat bottom.	AO4704-3 (Scanning Electron Microscopy image), item D; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AO4704-3 (Scanning Electron Microscopy image), item B; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO4704-5 (Secondary Ion Mass Spectroscopy data).)
5. The trenched field effect transistor of claim 1 wherein the heavy body comprises a heavily doped region having dopants of the second conductivity type at the abrupt junction.	The heavy body of the accused device is a heavily doped region of P-type dopants (a second conductivity type). (Fig. AO4704-3 (Scanning Electron Microscopy image), item E; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item E.)
6. The trenched field effect transistor of claim 5 wherein the heavily doped region is formed by implanting dopants of the second conductivity type at approximately the third depth.	The heavy body of the accused device is formed by implanting P-type dopants (a second conductivity type) in the doped well and extending to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AO4704-3 (Scanning Electron Microscopy image), item E; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item E.)
10. The trenched field effect transistor of claim 1 wherein the trench is lined with a dielectric layer and substantially filled with conductive material.	The trench of the accused device is lined with a dielectric layer and substantially filled with doped polysilicon (a conductive material). (Fig. AO4704-3 (Scanning Electron Microscopy image), items B and G; Fig. AO4704-4 (Scanning Capacitance Microscopy image), items B and G.)
11. The trenched field effect transistor of claim 10 wherein the conductive material comprises polysilicon.	The conductive material in the trench of the accused device is doped polysilicon. (Fig. AO4704-3 (Scanning Electron Microscopy image), item B; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item B.)
12. The trenched field effect transistor of claim 10 wherein the conductive material filling the trench is recessed relative to the surface of the semiconductor substrate.	The conductive polysilicon filling the trench of the accused device is recessed relative to the surface of the silicon semiconductor substrate. (Fig. AO4704-3 (Scanning Electron Microscopy image), item B; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item B.)

EXHIBIT 24

EXHIBIT 24

INFRINGEMENT OF U.S. PATENT NO. 6,710,406 B2

AOS AOD414 POWER MOSFET

CLAIM	AOD414 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AOD414 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AOD414-1 (datasheet); Fig. AOD414-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AOD414-1 (datasheet); Fig. AOD414-3 (Scanning Electron Microscopy image), item A; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending to a first depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. In the language of the claim, the predetermined depth to which the trench extends is a "first depth." (Fig. AOD414-3 (Scanning Electron Microscopy image), item B; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AOD414-3 (Scanning Electron Microscopy image), item C; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AOD414-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type, and formed into the substrate to a second depth that is less than said first depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well (a second depth) is less than the predetermined depth of the trench (a first depth). (Fig. AOD414-3 (Scanning Electron Microscopy image), item D; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item D.)
a heavy body formed in said doped well extending to a third depth that is less than said second depth of said doped well, the heavy body forming an abrupt junction with the well;	The accused device has a heavy body formed in the doped well that extends to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AOD414-3 (Scanning Electron Microscopy image), item E; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item E.) The junction between the doped P-type heavy body and the doped well is an abrupt junction. (Fig. AOD414-5 (Secondary Ion Mass Spectroscopy data).)
wherein, a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The location of the abrupt junction of the accused device is such that it creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench. (Fig. AOD414-5 (Secondary Ion Mass Spectroscopy data).)
2. The trenched field effect transistor of claim 1	The accused device has a doped well with a substantially flat bottom. (Fig.

CLAIM	AOD414 POWER MOSFET
wherein said doped well has a substantially flat bottom.	AOD414-3 (Scanning Electron Microscopy image), item D; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AOD414-3 (Scanning Electron Microscopy image), item B; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AOD414-5 (Secondary Ion Mass Spectroscopy data).)
5. The trenched field effect transistor of claim 1 wherein the heavy body comprises a heavily doped region having dopants of the second conductivity type at the abrupt junction.	The heavy body of the accused device is a heavily doped region of P-type dopants (a second conductivity type). (Fig. AOD414-3 (Scanning Electron Microscopy image), item E; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item E.)
6. The trenched field effect transistor of claim 5 wherein the heavily doped region is formed by implanting dopants of the second conductivity type at approximately the third depth.	The heavy body of the accused device is formed by implanting P-type dopants (a second conductivity type) in the doped well and extending to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AOD414-3 (Scanning Electron Microscopy image), item E; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item E.)
10. The trenched field effect transistor of claim 1 wherein the trench is lined with a dielectric layer and substantially filled with conductive material.	The trench of the accused device is lined with a dielectric layer and substantially filled with doped polysilicon (a conductive material). (Fig. AOD414-3 (Scanning Electron Microscopy image), items B and G; Fig. AOD414-4 (Scanning Capacitance Microscopy image), items B and G.)
11. The trenched field effect transistor of claim 10 wherein the conductive material comprises polysilicon.	The conductive material in the trench of the accused device is doped polysilicon. (Fig. AOD414-3 (Scanning Electron Microscopy image), item B; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item B.)
12. The trenched field effect transistor of claim 10 wherein the conductive material filling the trench is recessed relative to the surface of the semiconductor substrate.	The conductive polysilicon filling the trench of the accused device is recessed relative to the surface of the silicon semiconductor substrate. (Fig. AOD414-3 (Scanning Electron Microscopy image), item B; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item B.)

EXHIBIT 25

EXHIBIT 25

INFRINGEMENT OF U.S. PATENT NO. 6,710,406 B2

AOS AO4413A POWER MOSFET

CLAIM	AO4413A POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AO4413A Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AO4413A-1 (datasheet); Fig. AO4413A-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is a P-channel MOSFET, which is therefore formed on a substrate of doped P-type silicon. In the language of the claim, the P-type dopants in the substrate are a "first conductivity type." (Fig. AO4413A-1 (datasheet); Fig. AO4413A-3 (Scanning Electron Microscopy image), item A; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending to a first depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. In the language of the claim, the predetermined depth to which the trench extends is a "first depth." (Fig. AO4413A-3 (Scanning Electron Microscopy image), item B; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item C; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is a P-channel MOSFET, the source junctions (regions) are formed with P-type dopants, which are dopants of the first conductivity type. (Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type, and formed into the substrate to a second depth that is less than said first depth of the trench; and	The accused device has a lightly doped well formed with N-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well (a second depth) is less than the predetermined depth of the trench (a first depth). (Fig. AO4413A-3 (Scanning Electron Microscopy image), item D; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item D.)
a heavy body formed in said doped well extending to a third depth that is less than said second depth of said doped well, the heavy body forming an abrupt junction with the well;	The accused device has a heavy body formed in the doped well that extends to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AO4413A-3 (Scanning Electron Microscopy image), item E; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item E.) The junction between the doped N-type heavy body and the doped well is an abrupt junction. (Fig. AO4413A-5 (Secondary Ion Mass Spectroscopy data).)
wherein, a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The location of the abrupt junction of the accused device is such that it creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench. (Fig. AO4413A-5 (Secondary Ion Mass Spectroscopy data).)

CLAIM	AO4413A POWER MOSFET
2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item D; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item B; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO4413A-5 (Secondary Ion Mass Spectroscopy data).)
5. The trenched field effect transistor of claim 1 wherein the heavy body comprises a heavily doped region having dopants of the second conductivity type at the abrupt junction.	The heavy body of the accused device is a heavily doped region of N-type dopants (a second conductivity type). (Fig. AO4413A-3 (Scanning Electron Microscopy image), item E; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item E.)
6. The trenched field effect transistor of claim 5 wherein the heavily doped region is formed by implanting dopants of the second conductivity type at approximately the third depth.	The heavy body of the accused device is formed by implanting N-type dopants (a second conductivity type) in the doped well and extending to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AO4413A-3 (Scanning Electron Microscopy image), item E; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item E.)
10. The trenched field effect transistor of claim 1 wherein the trench is lined with a dielectric layer and substantially filled with conductive material.	The trench of the accused device is lined with a dielectric layer and substantially filled with doped polysilicon (a conductive material). (Fig. AO4413A-3 (Scanning Electron Microscopy image), items B and G; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), items B and G.)
11. The trenched field effect transistor of claim 10 wherein the conductive material comprises polysilicon.	The conductive material in the trench of the accused device is doped polysilicon. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item B; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item B.)
12. The trenched field effect transistor of claim 10 wherein the conductive material filling the trench is recessed relative to the surface of the semiconductor substrate.	The conductive polysilicon filling the trench of the accused device is recessed relative to the surface of the silicon semiconductor substrate. (Fig. AO4413A-3 (Scanning Electron Microscopy image), item B; Fig. AO4413A-4 (Scanning Capacitance Microscopy image), item B.)

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EXHIBIT 26

EXHIBIT 26

INFRINGEMENT OF U.S. PATENT NO. 6,710,406 B2

AOS AO6405 POWER MOSFET

CLAIM	AO6405 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AO6405 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AO6405-1 (datasheet); Fig. AO6405-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is a P-channel MOSFET, which is therefore formed on a substrate of doped P-type silicon. In the language of the claim, the P-type dopants in the substrate are a "first conductivity type." (Fig. AO6405-1 (datasheet); Fig. AO6405-3 (Scanning Electron Microscopy image), item A; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending to a first depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. In the language of the claim, the predetermined depth to which the trench extends is a "first depth." (Fig. AO6405-3 (Scanning Electron Microscopy image), item B; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO6405-3 (Scanning Electron Microscopy image), item C; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is a P-channel MOSFET, the source junctions (regions) are formed with P-type dopants, which are dopants of the first conductivity type. (Fig. AO6405-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type, and formed into the substrate to a second depth that is less than said first depth of the trench; and	The accused device has a lightly doped well formed with N-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well (a second depth) is less than the predetermined depth of the trench (a first depth). (Fig. AO6405-3 (Scanning Electron Microscopy image), item D; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item D.)
a heavy body formed in said doped well extending to a third depth that is less than said second depth of said doped well, the heavy body forming an abrupt junction with the well;	The accused device has a heavy body formed in the doped well that extends to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AO6405-3 (Scanning Electron Microscopy image), item E; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item E.) The junction between the doped N-type heavy body and the doped well is an abrupt junction. (Fig. AO6405-5 (Secondary Ion Mass Spectroscopy data).)
wherein, a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The location of the abrupt junction of the accused device is such that it creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench. (Fig. AO6405-5 (Secondary Ion Mass Spectroscopy data).)
2. The trenched field effect transistor of claim 1	The accused device has a doped well with a substantially flat bottom. (Fig.

CLAIM	AO6405 POWER MOSFET
wherein said doped well has a substantially flat bottom.	AO6405-3 (Scanning Electron Microscopy image), item D; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has a rounded top and bottom. (Fig. AO6405-3 (Scanning Electron Microscopy image), item B; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO6405-5 (Secondary Ion Mass Spectroscopy data).)
5. The trenched field effect transistor of claim 1 wherein the heavy body comprises a heavily doped region having dopants of the second conductivity type at the abrupt junction.	The heavy body of the accused device is a heavily doped region of N-type dopants (a second conductivity type). (Fig. AO6405-3 (Scanning Electron Microscopy image), item E; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item E.)
6. The trenched field effect transistor of claim 5 wherein the heavily doped region is formed by implanting dopants of the second conductivity type at approximately the third depth.	The heavy body of the accused device is formed by implanting N-type dopants (a second conductivity type) in the doped well and extending to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AO6405-3 (Scanning Electron Microscopy image), item E; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item E.)
10. The trenched field effect transistor of claim 1 wherein the trench is lined with a dielectric layer and substantially filled with conductive material.	The trench of the accused device is lined with a dielectric layer and substantially filled with doped polysilicon (a conductive material). (Fig. AO6405-3 (Scanning Electron Microscopy image), items B and G; Fig. AO6405-4 (Scanning Capacitance Microscopy image), items B and G.)
11. The trenched field effect transistor of claim 10 wherein the conductive material comprises polysilicon.	The conductive material in the trench of the accused device is doped polysilicon. (Fig. AO6405-3 (Scanning Electron Microscopy image), item B; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item B.)
12. The trenched field effect transistor of claim 10 wherein the conductive material filling the trench is recessed relative to the surface of the semiconductor substrate.	The conductive polysilicon filling the trench of the accused device is recessed relative to the surface of the silicon semiconductor substrate. (Fig. AO6405-3 (Scanning Electron Microscopy image), item B; Fig. AO6405-4 (Scanning Capacitance Microscopy image), item B.)

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EXHIBIT 27

EXHIBIT 27

INFRINGEMENT OF U.S. PATENT NO. 6,710,406 B2

AOS AO4912 POWER MOSFET

CLAIM	AO4912 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AO4912 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AO4912-1 (datasheet); Fig. AO4912-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4912-1 (datasheet); Fig. AO4912-3 (Scanning Electron Microscopy image), item A; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending to a first depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. In the language of the claim, the predetermined depth to which the trench extends is a "first depth." (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AO4912-3 (Scanning Electron Microscopy image), item C; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AO4912-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type, and formed into the substrate to a second depth that is less than said first depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well (a second depth) is less than the predetermined depth of the trench (a first depth). (Fig. AO4912-3 (Scanning Electron Microscopy image), item D; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item D.)
a heavy body formed in said doped well extending to a third depth that is less than said second depth of said doped well, the heavy body forming an abrupt junction with the well;	The accused device has a heavy body formed in the doped well that extends to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.) The junction between the doped P-type heavy body and the doped well is an abrupt junction. (Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).)
wherein, a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The location of the abrupt junction of the accused device is such that it creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench. (Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).)
2. The trenched field effect transistor of claim 1	The accused device has a doped well with a substantially flat bottom. (Fig.

CLAIM	AO4912 POWER MOSFET
wherein said doped well has a substantially flat bottom.	AO4912-3 (Scanning Electron Microscopy image), item D; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has rounded top and bottom corners. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).)
5. The trenched field effect transistor of claim 1 wherein the heavy body comprises a heavily doped region having dopants of the second conductivity type at the abrupt junction.	The heavy body of the accused device is a heavily doped region of P-type dopants (a second conductivity type) at the abrupt junction. (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.)
6. The trenched field effect transistor of claim 5 wherein the heavily doped region is formed by implanting dopants of the second conductivity type at approximately the third depth.	The heavy body of the accused device is formed by implanting P-type dopants (a second conductivity type) in the doped well and extending to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.)
10. The trenched field effect transistor of claim 1 wherein the trench is lined with a dielectric layer and substantially filled with conductive material.	The trench of the accused device is lined with a dielectric layer and substantially filled with doped polysilicon (a conductive material). (Fig. AO4912-3 (Scanning Electron Microscopy image), items B and G; Fig. AO4912-4 (Scanning Capacitance Microscopy image), items B and G.)
11. The trenched field effect transistor of claim 10 wherein the conductive material comprises polysilicon.	The conductive material in the trench of the accused device is doped polysilicon. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B.)
12. The trenched field effect transistor of claim 10 wherein the conductive material filling the trench is recessed relative to the surface of the semiconductor substrate.	The conductive polysilicon filling the trench of the accused device is recessed relative to the surface of the semiconductor substrate. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B.)
13. A field effect transistor comprising:	The accused device is a trenched field effect transistor. (Fig. AO4912-1 (datasheet); Fig. AO4912-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4912-1 (datasheet); Fig. AO4912-3 (Scanning Electron Microscopy image), item A; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item A.)
a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending to a first depth into said substrate, the space between adjacent trenches defining a contact area;	The accused device has gates formed using a striped design with substantially parallel trenches, with the trenches extending to a predetermined depth into the substrate and contact areas formed between the parallel trenches. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B; Fig. AO4912-8 (Scanning Electron Microscopy image (plan view), items B and C.)
a pair of doped source junctions positioned on opposite sides of each trench, the source junctions having dopants of the first conductivity type;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench and extending along the length of the trench. (Fig. AO4912-3 (Scanning Electron Microscopy image), item C; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item C; Fig. AO4912-

CLAIM	AO4912 POWER MOSFET
	8 (Scanning Electron Microscopy image (plan view), item A.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type.
a doped well having dopants of a second conductivity type with a charge opposite that of the first conductivity type, the doped well being formed in the semiconductor substrate between each pair of gate-forming trenches;	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate between each pair of gate-forming trenches. (Fig. AO4912-3 (Scanning Electron Microscopy image), item D; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item D.)
a heavy body formed inside the doped well and having a second depth that is less than the first depth of the trenches; and	The accused device has a highly doped heavy body formed with a higher concentration of P-type dopants (the second conductivity type) than the doped well, and the P-type heavy body extends to a depth in the substrate that is less than the depth of the trenches. (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.)
heavy body contact regions defined at the surface of the semiconductor substrate along the length of the contact area,	The accused device has heavy body contact areas on the surface of the semiconductor substrate along the length of the contact area. (Fig. AO4912-9 (Scanning Capacitance Microscopy image (plan view)), item B.)
wherein the heavy body forms an abrupt junction with the well, and the depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor.	The junction between the doped P-type heavy body and the doped well is an abrupt junction. (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.); Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).) The location of the abrupt junction is such that it creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.
14. The field effect transistor of claim 13, wherein each said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AO4912-3 (Scanning Electron Microscopy image), item D; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item D.)
15. The field effect transistor of claim 13 wherein the adjusted depth of the junction causes the breakdown origination point to occur approximately halfway between adjacent gate-forming trenches.	The depth of the abrupt junction in the accused device is selected to cause the breakdown origination point to occur approximately halfway between adjacent gate-forming trenches. (Fig. AO4912-5 (Secondary Ion Mass Spectroscopy data).)
16. The field effect transistor of claim 13 wherein each said doped well has a depth less than the first depth of said gate-forming trenches.	The accused device has a doped well formed at a depth less than the depth of the trenches. (Fig. AO4912-3 (Scanning Electron Microscopy image), items B and D; Fig. AO4912-4 (Scanning Capacitance Microscopy image), items B and D.)
17. The field effect transistor of claim 13 wherein each said gate-forming trench has rounded top and bottom corners.	The trench of the accused device has rounded top and bottom corners. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B.)
24. The field effect transistor of claim 13 wherein the heavy body forms a continuous doped region along substantially the entire length of said contact area.	The doped heavy body forms a continuous region along substantially the entire length of the contact area. (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.)
25. The field effect transistor of claim 13 wherein said doped source regions extend along the length of the trench.	The accused device has doped source regions extending along the length of the trench. (Fig. AO4912-8 (Scanning Capacitance Microscopy image (plan view)), item A.)
26. The field effect transistor of claim 25 further comprising a source contact region defined at the surface of the semiconductor substrate and configured to contacting the doped source regions.	The accused device has source contact regions located at the surface of the semiconductor substrate for contacting the doped source regions. (Fig. AO4912-9 (Scanning Capacitance Microscopy image (plan view)), item C.)

CLAIM	AO4912 POWER MOSFET
27. The field effect transistor of claim 25 further comprising a plurality of source contact regions disposed along the length of the contact area in an alternating fashion with the plurality of heavy body contact regions.	The accused device includes a plurality of source and heavy body contact regions which alternate along the length of the contact area. (Fig. AO4912-9 (Scanning Capacitance Microscopy image (plan view)), items A, B, C.)
28. The field effect transistor of claim 13 wherein between a pair of adjacent trenches, the heavy body is bounded by the pair of adjacent trenches and the doped source regions.	The accused device includes a heavy body bounded by a pair of adjacent trenches and doped source regions. (Fig. AO4912-3 (Scanning Electron Microscopy image), items B, C, E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), items B, C, E.)
29. The field effect transistor of claim 13 wherein between a pair of adjacent trenches, the heavy body extends continuously parallel to the longitudinal axis of the trenches.	The accused device includes a doped heavy body between a pair of adjacent trenches and extending continuously parallel to the longitudinal axis of the trenches. (Fig. AO4912-3 (Scanning Electron Microscopy image), item E; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item E.)
30. The field effect transistor of claim 13 further comprising:	
a layer of dielectric lining inside walls of each of said plurality of gate-forming trenches; and	The accused device includes a dielectric layer on the walls of each of the trenches. (Fig. AO4912-3 (Scanning Electron Microscopy image), item G; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item G.)
a layer of conductive material substantially filling the gate-forming trenches.	The accused device includes doped polysilicon which substantially fills the gate-forming trenches. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B.)
31. The field effect transistor of claim 30 wherein the layer of conductive material comprises polysilicon.	The accused device includes doped polysilicon (a conductive material) which substantially fills the gate-forming trenches. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B.)
32. The field effect transistor of claim 30 wherein the top surface of the layer of conductive material substantially filling the gate-forming trenches is recessed relative to the top surface of the semiconductor substrate.	The accused device includes doped polysilicon which substantially fills the gate-forming trenches. The top surface of the doped polysilicon in each gate-forming trench is recessed relative to the top surface of the semiconductor subtrate. (Fig. AO4912-3 (Scanning Electron Microscopy image), item B; Fig. AO4912-4 (Scanning Capacitance Microscopy image), item B.)

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EXHIBIT 28

EXHIBIT 28

INFRINGEMENT OF U.S. PATENT NO. 6,710,406 B2

AOS AOD438 POWER MOSFET

CLAIM	AOD438 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AOD438 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AOD438-1 (datasheet); Fig. AOD438-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AOD438-1 (datasheet); Fig. AOD438-3 (Scanning Electron Microscopy image), item A; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending to a first depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. In the language of the claim, the predetermined depth to which the trench extends is a "first depth." (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AOD438-3 (Scanning Electron Microscopy image), item C; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AOD438-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type, and formed into the substrate to a second depth that is less than said first depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well (a second depth) is less than the predetermined depth of the trench (a first depth). (Fig. AOD438-3 (Scanning Electron Microscopy image), item D; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item D.)
a heavy body formed in said doped well extending to a third depth that is less than said second depth of said doped well, the heavy body forming an abrupt junction with the well;	The accused device has a heavy body formed in the doped well that extends to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.) The junction between the doped P-type heavy body and the doped well is an abrupt junction. (Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).)
wherein, a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The location of the abrupt junction of the accused device is such that it creates a peak electric field when voltage is applied to the accused device; and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench. (Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).)
2. The trenched field effect transistor of claim 1	The accused device has a doped well with a substantially flat bottom. (Fig.

CLAIM	AOD438 POWER MOSFET
wherein said doped well has a substantially flat bottom.	AOD438-3 (Scanning Electron Microscopy image), item D; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has rounded top and bottom corners. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).)
5. The trenched field effect transistor of claim 1 wherein the heavy body comprises a heavily doped region having dopants of the second conductivity type at the abrupt junction.	The heavy body of the accused device is a heavily doped region of P-type dopants (a second conductivity type) at the abrupt junction. (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.)
6. The trenched field effect transistor of claim 5 wherein the heavily doped region is formed by implanting dopants of the second conductivity type at approximately the third depth.	The heavy body of the accused device is formed by implanting P-type dopants (a second conductivity type) in the doped well and extending to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.)
10. The trenched field effect transistor of claim 1 wherein the trench is lined with a dielectric layer and substantially filled with conductive material.	The trench of the accused device is lined with a dielectric layer and substantially filled with doped polysilicon (a conductive material). (Fig. AOD438-3 (Scanning Electron Microscopy image), items B and G; Fig. AOD438-4 (Scanning Capacitance Microscopy image), items B and G.)
11. The trenched field effect transistor of claim 10 wherein the conductive material comprises polysilicon.	The conductive material in the trench of the accused device is doped polysilicon. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B.)
12. The trenched field effect transistor of claim 10 wherein the conductive material filling the trench is recessed relative to the surface of the semiconductor substrate.	The conductive polysilicon filling the trench of the accused device is recessed relative to the surface of the semiconductor substrate. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B.)
13. A field effect transistor comprising:	The accused device is a trenched field effect transistor. (Fig. AOD438-1 (datasheet); Fig. AOD438-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AOD438-1 (datasheet); Fig. AOD438-3 (Scanning Electron Microscopy image), item A; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item A.)
a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending to a first depth into said substrate, the space between adjacent trenches defining a contact area;	The accused device has gates formed using a striped design with substantially parallel trenches, with the trenches extending to a predetermined depth into the substrate and contact areas formed between the parallel trenches. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B; Fig. AOD438-8 (Scanning Electron Microscopy image (plan view), items B and C.)
a pair of doped source junctions positioned on opposite sides of each trench, the source junctions having dopants of the first conductivity type;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench and extending along the length of the trench. (Fig. AOD438-3 (Scanning Electron Microscopy image), item C; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item C; Fig.

CLAIM	AOD438 POWER MOSFET
	AOD438-8 (Scanning Electron Microscopy image (plan view), item A.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type.
a doped well having dopants of a second conductivity type with a charge opposite that of the first conductivity type, the doped well being formed in the semiconductor substrate between each pair of gate-forming trenches;	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate between each pair of gate-forming trenches. (Fig. AOD438-3 (Scanning Electron Microscopy image), item D; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item D.)
a heavy body formed inside the doped well and having a second depth that is less than the first depth of the trenches; and	The accused device has a highly doped heavy body formed with a higher concentration of P-type dopants (the second conductivity type) than the doped well, and the P-type heavy body extends to a depth in the substrate that is less than the depth of the trenches. (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.)
heavy body contact regions defined at the surface of the semiconductor substrate along the length of the contact area,	The accused device has heavy body contact areas on the surface of the semiconductor substrate along the length of the contact area. (Fig. AOD438-9 (Scanning Capacitance Microscopy image (plan view)), item B.)
wherein the heavy body forms an abrupt junction with the well, and the depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor.	The junction between the doped P-type heavy body and the doped well is an abrupt junction. (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.); Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).) The location of the abrupt junction is such that it creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.
14. The field effect transistor of claim 13, wherein each said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AOD438-3 (Scanning Electron Microscopy image), item D; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item D.)
15. The field effect transistor of claim 13 wherein the adjusted depth of the junction causes the breakdown origination point to occur approximately halfway between adjacent gate-forming trenches.	The depth of the abrupt junction in the accused device is selected to cause the breakdown origination point to occur approximately halfway between adjacent gate-forming trenches. (Fig. AOD438-5 (Secondary Ion Mass Spectroscopy data).)
16. The field effect transistor of claim 13 wherein each said doped well has a depth less than the first depth of said gate-forming trenches.	The accused device has a doped well formed at a depth less than the depth of the trenches. (Fig. AOD438-3 (Scanning Electron Microscopy image), items B and D; Fig. AOD438-4 (Scanning Capacitance Microscopy image), items B and D.)
17. The field effect transistor of claim 13 wherein each said gate-forming trench has rounded top and bottom corners.	The trench of the accused device has rounded top and bottom corners. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B.)
24. The field effect transistor of claim 13 wherein the heavy body forms a continuous doped region along substantially the entire length of said contact area.	The doped heavy body forms a continuous region along substantially the entire length of the contact area. (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.)
25. The field effect transistor of claim 13 wherein said doped source regions extend along the length of the trench.	The accused device has doped source regions extending along the length of the trench. (Fig. AOD438-8 (Scanning Capacitance Microscopy image (plan view)), item A.)
26. The field effect transistor of claim 25 further comprising a source contact region defined at the surface of the semiconductor substrate and configured to contacting the doped source regions.	The accused device has source contact regions located at the surface of the semiconductor substrate for contacting the doped source regions. (Fig. AOD438-9 (Scanning Capacitance Microscopy image (plan view)), item C.)

CLAIM	AOD438 POWER MOSFET
27. The field effect transistor of claim 25 further comprising a plurality of source contact regions disposed along the length of the contact area in an alternating fashion with the plurality of heavy body contact regions.	The accused device includes a plurality of source and heavy body contact regions which alternate along the length of the contact area. (Fig. AOD438-9 (Scanning Capacitance Microscopy image (plan view)), items A, B, C.)
28. The field effect transistor of claim 13 wherein between a pair of adjacent trenches, the heavy body is bounded by the pair of adjacent trenches and the doped source regions.	The accused device includes a heavy body bounded by a pair of adjacent trenches and doped source regions. (Fig. AOD438-3 (Scanning Electron Microscopy image), items B, C, E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), items B, C, E.)
29. The field effect transistor of claim 13 wherein between a pair of adjacent trenches, the heavy body extends continuously parallel to the longitudinal axis of the trenches.	The accused device includes a doped heavy body between a pair of adjacent trenches and extending continuously parallel to the longitudinal axis of the trenches. (Fig. AOD438-3 (Scanning Electron Microscopy image), item E; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item E.)
30. The field effect transistor of claim 13 further comprising:	
a layer of dielectric lining inside walls of each of said plurality of gate-forming trenches; and	The accused device includes a dielectric layer on the walls of each of the trenches. (Fig. AOD438-3 (Scanning Electron Microscopy image), item G; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item G.)
a layer of conductive material substantially filling the gate-forming trenches.	The accused device includes doped polysilicon which substantially fills the gate-forming trenches. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B.)
31. The field effect transistor of claim 30 wherein the layer of conductive material comprises polysilicon.	The accused device includes doped polysilicon (a conductive material) which substantially fills the gate-forming trenches. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B.)
32. The field effect transistor of claim 30 wherein the top surface of the layer of conductive material substantially filling the gate-forming trenches is recessed relative to the top surface of the semiconductor substrate.	The accused device includes doped polysilicon which substantially fills the gate-forming trenches. The top surface of the doped polysilicon in each gate-forming trench is recessed relative to the top surface of the semiconductor subtrate. (Fig. AOD438-3 (Scanning Electron Microscopy image), item B; Fig. AOD438-4 (Scanning Capacitance Microscopy image), item B.)

EXHIBIT 29

EXHIBIT 29

INFRINGEMENT OF U.S. PATENT NO. 6,710,406 B2

AOS AOL1414 POWER MOSFET

CLAIM	AOL1414 POWER MOSFET
1. A trenched field effect transistor comprising:	The AOS AOL1414 Power MOSFET ("the accused device") is a trenched field effect transistor. (Fig. AOL1414-1 (datasheet); Fig. AOL1414-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AOL1414-1 (datasheet); Fig. AOL1414-3 (Scanning Electron Microscopy image), item A; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item A.)
a trench extending to a first depth into said semiconductor substrate;	The accused device has a trench extending to a predetermined depth into the substrate. In the language of the claim, the predetermined depth to which the trench extends is a "first depth." (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B.)
a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item C; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item C.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type. (Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item C.)
a doped well having dopants of a second conductivity type, and formed into the substrate to a second depth that is less than said first depth of the trench; and	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate, and the depth of the doped well (a second depth) is less than the predetermined depth of the trench (a first depth). (Fig. AOL1414-3 (Scanning Electron Microscopy image), item D; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item D.)
a heavy body formed in said doped well extending to a third depth that is less than said second depth of said doped well, the heavy body forming an abrupt junction with the well;	The accused device has a heavy body formed in the doped well that extends to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.) The junction between the doped P-type heavy body and the doped well is an abrupt junction. (Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).)
wherein, a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.	The location of the abrupt junction of the accused device is such that it creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench. (Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).)
2. The trenched field effect transistor of claim 1	The accused device has a doped well with a substantially flat bottom. (Fig.

CLAIM	AOL1414 POWER MOSFET
wherein said doped well has a substantially flat bottom.	AOL1414-3 (Scanning Electron Microscopy image), item D; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item D.)
3. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.	The trench of the accused device has rounded top and bottom corners. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B.)
4. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.	The abrupt junction in the accused device creates a peak electric field in the area of the junction when voltage is applied, so that the transistor breakdown initiation point occurs in the area of the abrupt junction. (Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).)
5. The trenched field effect transistor of claim 1 wherein the heavy body comprises a heavily doped region having dopants of the second conductivity type at the abrupt junction.	The heavy body of the accused device is a heavily doped region of P-type dopants (a second conductivity type) at the abrupt junction. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.)
6. The trenched field effect transistor of claim 5 wherein the heavily doped region is formed by implanting dopants of the second conductivity type at approximately the third depth.	The heavy body of the accused device is formed by implanting P-type dopants (a second conductivity type) in the doped well and extending to a depth (a third depth) that is less than the depth of the well (a second depth). (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.)
10. The trenched field effect transistor of claim 1 wherein the trench is lined with a dielectric layer and substantially filled with conductive material.	The trench of the accused device is lined with a dielectric layer and substantially filled with doped polysilicon (a conductive material). (Fig. AOL1414-3 (Scanning Electron Microscopy image), items B and G; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), items B and G.)
11. The trenched field effect transistor of claim 10 wherein the conductive material comprises polysilicon.	The conductive material in the trench of the accused device is doped polysilicon. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B.)
12. The trenched field effect transistor of claim 10 wherein the conductive material filling the trench is recessed relative to the surface of the semiconductor substrate.	The conductive polysilicon filling the trench of the accused device is recessed relative to the surface of the semiconductor substrate. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B.)
13. A field effect transistor comprising:	The accused device is a trenched field effect transistor. (Fig. AOL1414-1 (datasheet); Fig. AOL1414-2 (package marking).)
a semiconductor substrate having dopants of a first conductivity type;	The accused device is an N-channel MOSFET, which is therefore formed on a substrate of doped N-type silicon. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AOL1414-1 (datasheet); Fig. AOL1414-3 (Scanning Electron Microscopy image), item A; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item A.)
a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending to a first depth into said substrate, the space between adjacent trenches defining a contact area;	The accused device has gates formed using a striped design with substantially parallel trenches, with the trenches extending to a predetermined depth into the substrate and contact areas formed between the parallel trenches. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B; Fig. AOL1414-8 (Scanning Electron Microscopy image (plan view), items B and C.)
a pair of doped source junctions positioned on opposite sides of each trench, the source junctions having dopants of the first conductivity type;	The accused device has a pair of source junctions (regions) positioned on opposite sides of the trench and extending along the length of the trench. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item C; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item C; Fig.

CLAIM	AOL1414 POWER MOSFET
	AOL1414-8 (Scanning Electron Microscopy image (plan view), item A.) Because the accused device is an N-channel MOSFET, the source junctions (regions) are formed with N-type dopants, which are dopants of the first conductivity type.
a doped well having dopants of a second conductivity type with a charge opposite that of the first conductivity type, the doped well being formed in the semiconductor substrate between each pair of gate-forming trenches;	The accused device has a lightly doped well formed with P-type dopants (a second conductivity type opposite to the first conductivity type) that is formed in the substrate between each pair of gate-forming trenches. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item D; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item D.)
a heavy body formed inside the doped well and having a second depth that is less than the first depth of the trenches; and	The accused device has a highly doped heavy body formed with a higher concentration of P-type dopants (the second conductivity type) than the doped well, and the P-type heavy body extends to a depth in the substrate that is less than the depth of the trenches. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.)
heavy body contact regions defined at the surface of the semiconductor substrate along the length of the contact area,	The accused device has heavy body contact areas on the surface of the semiconductor substrate along the length of the contact area. (Fig. AOL1414-9 (Scanning Capacitance Microscopy image (plan view)), item B.)
wherein the heavy body forms an abrupt junction with the well, and the depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor.	The junction between the doped P-type heavy body and the doped well is an abrupt junction. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.); Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).) The location of the abrupt junction is such that it creates a peak electric field when voltage is applied to the accused device, and the depth of this abrupt junction relative to the depth of the well is such that the peak electric field causes the breakdown initiation point to be spaced away from the trench.
14. The field effect transistor of claim 13, wherein each said doped well has a substantially flat bottom.	The accused device has a doped well with a substantially flat bottom. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item D; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item D.)
15. The field effect transistor of claim 13 wherein the adjusted depth of the junction causes the breakdown origination point to occur approximately halfway between adjacent gate-forming trenches.	The depth of the abrupt junction in the accused device is selected to cause the breakdown origination point to occur approximately halfway between adjacent gate-forming trenches. (Fig. AOL1414-5 (Secondary Ion Mass Spectroscopy data).)
16. The field effect transistor of claim 13 wherein each said doped well has a depth less than the first depth of said gate-forming trenches.	The accused device has a doped well formed at a depth less than the depth of the trenches. (Fig. AOL1414-3 (Scanning Electron Microscopy image), items B and D; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), items B and D.)
17. The field effect transistor of claim 13 wherein each said gate-forming trench has rounded top and bottom corners.	The trench of the accused device has rounded top and bottom corners. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B.)
24. The field effect transistor of claim 13 wherein the heavy body forms a continuous doped region along substantially the entire length of said contact area.	The doped heavy body forms a continuous region along substantially the entire length of the contact area. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.)
25. The field effect transistor of claim 13 wherein said doped source regions extend along the length of the trench.	The accused device has doped source regions extending along the length of the trench. (Fig. AOL1414-8 (Scanning Capacitance Microscopy image (plan view)), item A.)
26. The field effect transistor of claim 25 further comprising a source contact region defined at the surface of the semiconductor substrate and configured to contacting the doped source regions.	The accused device has source contact regions located at the surface of the semiconductor substrate for contacting the doped source regions. (Fig. AOL1414-9 (Scanning Capacitance Microscopy image (plan view)), item C.)

CLAIM	AOL1414 POWER MOSFET
27. The field effect transistor of claim 25 further comprising a plurality of source contact regions disposed along the length of the contact area in an alternating fashion with the plurality of heavy body contact regions.	The accused device includes a plurality of source and heavy body contact regions which alternate along the length of the contact area. (Fig. AOL1414-9 (Scanning Capacitance Microscopy image (plan view)), items A, B, C.)
28. The field effect transistor of claim 13 wherein between a pair of adjacent trenches, the heavy body is bounded by the pair of adjacent trenches and the doped source regions.	The accused device includes a heavy body bounded by a pair of adjacent trenches and doped source regions. (Fig. AOL1414-3 (Scanning Electron Microscopy image), items B, C, E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), items B, C, E.)
29. The field effect transistor of claim 13 wherein between a pair of adjacent trenches, the heavy body extends continuously parallel to the longitudinal axis of the trenches.	The accused device includes a doped heavy body between a pair of adjacent trenches and extending continuously parallel to the longitudinal axis of the trenches. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item E; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item E.)
30. The field effect transistor of claim 13 further comprising:	
a layer of dielectric lining inside walls of each of said plurality of gate-forming trenches; and	The accused device includes a dielectric layer on the walls of each of the trenches. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item G; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item G.)
a layer of conductive material substantially filling the gate-forming trenches.	The accused device includes doped polysilicon which substantially fills the gate-forming trenches. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B.)
31. The field effect transistor of claim 30 wherein the layer of conductive material comprises polysilicon.	The accused device includes doped polysilicon (a conductive material) which substantially fills the gate-forming trenches. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B.)
32. The field effect transistor of claim 30 wherein the top surface of the layer of conductive material substantially filling the gate-forming trenches is recessed relative to the top surface of the semiconductor substrate.	The accused device includes doped polysilicon which substantially fills the gate-forming trenches. The top surface of the doped polysilicon in each gate-forming trench is recessed relative to the top surface of the semiconductor subtrate. (Fig. AOL1414-3 (Scanning Electron Microscopy image), item B; Fig. AOL1414-4 (Scanning Capacitance Microscopy image), item B.)

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EXHIBIT 30

EXHIBIT 30

INFRINGEMENT OF U.S. PATENT NO. 6,828,195

AOS AO4812 POWER MOSFET

CLAIM	AO4812 POWER MOSFET
1. A method of manufacturing a trench transistor comprising:	The AOS AO4812 Power MOSFET is a trenched field effect transistor. (Fig. AO4812-1 (datasheet); Fig. AO4812-2 (package marking).) The method used to manufacture the AO4812 power MOSFET is, by definition, a method of manufacturing a trench transistor ("the accused method").
providing a semiconductor substrate having dopants of a first conductivity type;	The accused method includes the use of a silicon semiconductor substrate with N-type dopants. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4812-1 (datasheet); Fig. AO4812-3 (Scanning Electron Microscopy image), item A; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches extending to a first depth into the semiconductor substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO4812-3 (Scanning Electron Microscopy image), item B; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item B.)
lining each of the plurality of trenches with a gate dielectric material;	The accused method includes lining each trench with a dielectric layer. (Fig. AO4812-3 (Scanning Electron Microscopy image), item G; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling each dielectric-lined trench with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AO4812-3 (Scanning Electron Microscopy image), item B; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item B.)
forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AO4812-3 (Scanning Electron Microscopy image), item D; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body extending inside the doped well to a third depth that is less than said second depth of said doped well, the heavy body having dopants of the second conductivity type and forming an abrupt junction with the	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AO4812-3 (Scanning Electron

CLAIM	AO4812 POWER MOSFET
well;	Microscopy image), item E; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item E.) The change in concentration between the heavy body and the doped well forms an abrupt junction. (Fig. AO4812-5 (Secondary Ion Mass Spectroscopy data).)
and forming a source region inside the well, the source region having dopants of the first conductivity types.	The accused method includes creating a source region inside the well, adjacent to the trench, having N-type dopants (a first conductivity type). (Fig. AO4812-3 (Scanning Electron Microscopy image), item C; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item C.)
2. The method of claim 1 wherein the step of forming a doped well forms the well with a substantially flat bottom.	The doped well created by the accused method has a substantially flat bottom. (Fig. AO4812-3 (Scanning Electron Microscopy image), item D; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item D.)
6. The method of claim 1 wherein the step of substantially filling each dielectric-lined trench leaves a recess at an upper portion of each trench.	The step of the accused method in which the dielectric-lined trench is substantially filled with conductive polysilicon includes leaving a recess at the upper portion of each trench. (Fig. AO4812-3 (Scanning Electron Microscopy image), item B; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item B.)
7. The method of claim 6 further comprising filling the recess at the upper portion of each trench with dielectric material.	The accused method includes filling the recess at the upper portion of the trench with dielectric material. (Fig. AO4812-3 (Scanning Electron Microscopy image), item B; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item B.)
8. The method of claim 1 wherein the step of forming the heavy body comprises a double implant process.	The step of the accused method in which the P-doped heavy body is created in the P-doped well includes two implants of P-type dopants (a double implant process). (Fig. AO4812-5 (Secondary Ion Mass Spectroscopy data).)
9. The method of claim 8 wherein the double implant process comprises:	
a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body;	The accused method includes a first implant of dopants of the second conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body. (Fig. AO4812-5 (Secondary Ion Mass Spectroscopy data).)
and a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.	The accused method includes a second implant of dopants of the second conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body. (Fig. AO4812-5 (Secondary Ion Mass Spectroscopy data).)
10. The method of claim 9 wherein the first implant occurs at approximately the third depth.	The first implant of the accused method occurs at approximately the third depth. (Fig. AO4812-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of claim 9 wherein the first energy level is higher than the second energy level.	In the accused method, the first energy level is higher than the second energy level. (Fig. AO4812-5 (Secondary Ion Mass

CLAIM	AO4812 POWER MOSFET
	Spectroscopy data).)
12. The method of claim 11 wherein the first dosage is higher than the second dosage.	In the accused method, the first dosage is higher than the second dosage. (Fig. AO4812-5 (Secondary Ion Mass Spectroscopy data).)
13. The method of claim 1 wherein the step of forming the heavy body comprises a process of diffusing dopants of the second conductivity type.	The step of the accused method in which the P-type heavy body is created includes a process in which P-type dopants (a second conductivity type) are diffused into the P-doped well. (Fig. AO4812-3 (Scanning Electron Microscopy image), item E; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item E.)
21. A method of manufacturing a trench field effect transistor on a semiconductor substrate having dopants of a first conductivity type, the method comprising:	The accused method includes making a trench field effect transistor on a silicon semiconductor substrate created with N-type dopants (a first conductivity type). (Fig. AO4812-3 (Scanning Electron Microscopy image), item A; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item A.)
etching a plurality of trenches into the semiconductor substrate to a first depth;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO4812-3 (Scanning Electron Microscopy image), item B; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item B.)
lining the plurality of trenches with dielectric layer;	The accused method includes lining each trench with a dielectric layer. (Fig. AO4812-3 (Scanning Electron Microscopy image), item G; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling the dielectric-lined plurality of trenches with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AO4812-3 (Scanning Electron Microscopy image), item B; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item B.)
forming a well between adjacent trenches to a second depth that is shallower than the first depth, the well having dopants of second conductivity type opposite to the first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate between adjacent trenches that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AO4812-3 (Scanning Electron Microscopy image), item D; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body inside the well to a third depth that is shallower than the second depth, the heavy body having dopants of the second conductivity type;	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AO4812-3 (Scanning Electron Microscopy image), item E; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item E.)

CLAIM	AO4812 POWER MOSFET
and forming a source region inside the well and adjacent to trenches, the source region having dopants of the first conductivity type, wherein, the step of forming a heavy body employs a process to form an abrupt junction between the heavy body and the well at approximately the third depth.	The accused method includes creating an N-type doped source region (a first conductivity type) inside the well and adjacent to trenches. (Fig. AO4812-3 (Scanning Electron Microscopy image), item C; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item C.) The accused method creates a change in the concentrations between the heavy body and the doped well, which forms an abrupt junction between the heavy body and the doped well at approximately the depth of the heavy body (a third depth). (Fig. AO4812-5 (Secondary Ion Mass Spectroscopy data).)
22. The method of claim 21 further comprising adjusting a location of the abrupt junction relative to the depth of the well so that a transistor breakdown current is spaced away from the trench in the semiconductor.	The depth of the abrupt junction created by the accused method is positioned relative to the depth of the well such that the peak electric field causes transistor breakdown current to be spaced away from the trench. (Fig. AO4812-3 (Scanning Electron Microscopy image), item E; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4812-5 (Secondary Ion Mass Spectroscopy data).)

EXHIBIT 31

EXHIBIT 31

INFRINGEMENT OF U.S. PATENT NO. 6,828,195

AOS AO4468 POWER MOSFET

CLAIM	AO4468 POWER MOSFET
1. A method of manufacturing a trench transistor comprising:	The AOS AO4468 Power MOSFET is a trenched field effect transistor. (Fig. AO4468-1 (datasheet); Fig. AO4468-2 (package marking).) The method used to manufacture the AO4468 power MOSFET is, by definition, a method of manufacturing a trench transistor ("the accused method").
providing a semiconductor substrate having dopants of a first conductivity type;	The accused method includes the use of a silicon semiconductor substrate with N-type dopants. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4468-1 (datasheet); Fig. AO4468-3 (Scanning Electron Microscopy image), item A; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches extending to a first depth into the semiconductor substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO4468-3 (Scanning Electron Microscopy image), item B; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item B.)
lining each of the plurality of trenches with a gate dielectric material;	The accused method includes lining each trench with a dielectric layer. (Fig. AO4468-3 (Scanning Electron Microscopy image), item G; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling each dielectric-lined trench with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AO4468-3 (Scanning Electron Microscopy image), item B; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item B.)
forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AO4468-3 (Scanning Electron Microscopy image), item D; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body extending inside the doped well to a third depth that is less than said second depth of said doped well, the heavy body having dopants of the second conductivity type and forming an abrupt junction with the	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AO4468-3 (Scanning Electron

CLAIM	AO4468 POWER MOSFET
well;	Microscopy image), item E; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item E.) The change in concentration between the heavy body and the doped well forms an abrupt junction. (Fig. AO4468-5 (Secondary Ion Mass Spectroscopy data).)
and forming a source region inside the well, the source region having dopants of the first conductivity types.	The accused method includes creating a source region inside the well, adjacent to the trench, having N-type dopants (a first conductivity type). (Fig. AO4468-3 (Scanning Electron Microscopy image), item C; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item C.)
2. The method of claim 1 wherein the step of forming a doped well forms the well with a substantially flat bottom.	The doped well created by the accused method has a substantially flat bottom. (Fig. AO4468-3 (Scanning Electron Microscopy image), item D; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item D.)
6. The method of claim 1 wherein the step of substantially filling each dielectric-lined trench leaves a recess at an upper portion of each trench.	The step of the accused method in which the dielectric-lined trench is substantially filled with conductive polysilicon includes leaving a recess at the upper portion of each trench. (Fig. AO4468-3 (Scanning Electron Microscopy image), item B; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item B.)
7. The method of claim 6 further comprising filling the recess at the upper portion of each trench with dielectric material.	The accused method includes filling the recess at the upper portion of the trench with dielectric material. (Fig. AO4468-3 (Scanning Electron Microscopy image), item B; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item B.)
8. The method of claim 1 wherein the step of forming the heavy body comprises a double implant process.	The step of the accused method in which the P-doped heavy body is created in the P-doped well includes two implants of P-type dopants (a double implant process). (Fig. AO4468-5 (Secondary Ion Mass Spectroscopy data).)
9. The method of claim 8 wherein the double implant process comprises:	
a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body;	The accused method includes a first implant of dopants of the second conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body. (Fig. AO4468-5 (Secondary Ion Mass Spectroscopy data).)
and a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.	The accused method includes a second implant of dopants of the second conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body. (Fig. AO4468-5 (Secondary Ion Mass Spectroscopy data).)
10. The method of claim 9 wherein the first implant occurs at approximately the third depth.	The first implant of the accused method occurs at approximately the third depth. (Fig. AO4468-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of claim 9 wherein the first energy level is higher than the second energy level.	In the accused method, the first energy level is higher than the second energy level. (Fig. AO4468-5 (Secondary Ion Mass

CLAIM	AO4468 POWER MOSFET
	Spectroscopy data).)
12. The method of claim 11 wherein the first dosage is higher than the second dosage.	In the accused method, the first dosage is higher than the second dosage. (Fig. AO4468-5 (Secondary Ion Mass Spectroscopy data).)
13. The method of claim 1 wherein the step of forming the heavy body comprises a process of diffusing dopants of the second conductivity type.	The step of the accused method in which the P-type heavy body is created includes a process in which P-type dopants (a second conductivity type) are diffused into the P-doped well. (Fig. AO4468-3 (Scanning Electron Microscopy image), item E; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item E.)
21. A method of manufacturing a trench field effect transistor on a semiconductor substrate having dopants of a first conductivity type, the method comprising:	The accused method includes making a trench field effect transistor on a silicon semiconductor substrate created with N-type dopants (a first conductivity type). (Fig. AO4468-3 (Scanning Electron Microscopy image), item A; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item A.)
etching a plurality of trenches into the semiconductor substrate to a first depth;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO4468-3 (Scanning Electron Microscopy image), item B; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item B.)
lining the plurality of trenches with dielectric layer;	The accused method includes lining each trench with a dielectric layer. (Fig. AO4468-3 (Scanning Electron Microscopy image), item G; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling the dielectric-lined plurality of trenches with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AO4468-3 (Scanning Electron Microscopy image), item B; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item B.)
forming a well between adjacent trenches to a second depth that is shallower than the first depth, the well having dopants of second conductivity type opposite to the first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate between adjacent trenches that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AO4468-3 (Scanning Electron Microscopy image), item D; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body inside the well to a third depth that is shallower than the second depth, the heavy body having dopants of the second conductivity type;	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AO4468-3 (Scanning Electron Microscopy image), item E; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item E.)

CLAIM	AO4468 POWER MOSFET
and forming a source region inside the well and adjacent to trenches, the source region having dopants of the first conductivity type, wherein, the step of forming a heavy body employs a process to form an abrupt junction between the heavy body and the well at approximately the third depth.	The accused method includes creating an N-type doped source region (a first conductivity type) inside the well and adjacent to trenches. (Fig. AO4468-3 (Scanning Electron Microscopy image), item C; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item C.) The accused method creates a change in the concentrations between the heavy body and the doped well, which forms an abrupt junction between the heavy body and the doped well at approximately the depth of the heavy body (a third depth). (Fig. AO4468-5 (Secondary Ion Mass Spectroscopy data).)
22. The method of claim 21 further comprising adjusting a location of the abrupt junction relative to the depth of the well so that a transistor breakdown current is spaced away from the trench in the semiconductor.	The depth of the abrupt junction created by the accused method is positioned relative to the depth of the well such that the peak electric field causes transistor breakdown current to be spaced away from the trench. (Fig. AO4468-3 (Scanning Electron Microscopy image), item E; Fig. AO4468-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4468-5 (Secondary Ion Mass Spectroscopy data).)

EXHIBIT 32

EXHIBIT 32

INFRINGEMENT OF U.S. PATENT NO. 6,828,195

AOS AO6402 POWER MOSFET

CLAIM	AO6402 POWER MOSFET
1. A method of manufacturing a trench transistor comprising:	The AOS AO6402 Power MOSFET is a trenched field effect transistor. (Fig. AO6402-1 (datasheet); Fig. AO6402-2 (package marking).) The method used to manufacture the AO6402 power MOSFET is, by definition, a method of manufacturing a trench transistor ("the accused method").
providing a semiconductor substrate having dopants of a first conductivity type;	The accused method includes the use of a silicon semiconductor substrate with N-type dopants. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO6402-1 (datasheet); Fig. AO6402-3 (Scanning Electron Microscopy image), item A; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches extending to a first depth into the semiconductor substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO6402-3 (Scanning Electron Microscopy image), item B; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item B.)
lining each of the plurality of trenches with a gate dielectric material;	The accused method includes lining each trench with a dielectric layer. (Fig. AO6402-3 (Scanning Electron Microscopy image), item G; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling each dielectric-lined trench with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AO6402-3 (Scanning Electron Microscopy image), item B; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item B.)
forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AO6402-3 (Scanning Electron Microscopy image), item D; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body extending inside the doped well to a third depth that is less than said second depth of said doped well, the heavy body having dopants of the second conductivity type and forming an abrupt junction with the	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AO6402-3 (Scanning Electron

CLAIM	AO6402 POWER MOSFET
well;	Microscopy image), item E; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item E.) The change in concentration between the heavy body and the doped well forms an abrupt junction. (Fig. AO6402-5 (Secondary Ion Mass Spectroscopy data).)
and forming a source region inside the well, the source region having dopants of the first conductivity types.	The accused method includes creating a source region inside the well, adjacent to the trench, having N-type dopants (a first conductivity type). (Fig. AO6402-3 (Scanning Electron Microscopy image), item C; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item C.)
2. The method of claim 1 wherein the step of forming a doped well forms the well with a substantially flat bottom.	The doped well created by the accused method has a substantially flat bottom. (Fig. AO6402-3 (Scanning Electron Microscopy image), item D; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item D.)
6. The method of claim 1 wherein the step of substantially filling each dielectric-lined trench leaves a recess at an upper portion of each trench.	The step of the accused method in which the dielectric-lined trench is substantially filled with conductive polysilicon includes leaving a recess at the upper portion of each trench. (Fig. AO6402-3 (Scanning Electron Microscopy image), item B; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item B.)
7. The method of claim 6 further comprising filling the recess at the upper portion of each trench with dielectric material.	The accused method includes filling the recess at the upper portion of the trench with dielectric material. (Fig. AO6402-3 (Scanning Electron Microscopy image), item B; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item B.)
8. The method of claim 1 wherein the step of forming the heavy body comprises a double implant process.	The step of the accused method in which the P-doped heavy body is created in the P-doped well includes two implants of P-type dopants (a double implant process). (Fig. AO6402-5 (Secondary Ion Mass Spectroscopy data).)
9. The method of claim 8 wherein the double implant process comprises:	
a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body;	The accused method includes a first implant of dopants of the second conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body. (Fig. AO6402-5 (Secondary Ion Mass Spectroscopy data).)
and a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.	The accused method includes a second implant of dopants of the second conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body. (Fig. AO6402-5 (Secondary Ion Mass Spectroscopy data).)
10. The method of claim 9 wherein the first implant occurs at approximately the third depth.	The first implant of the accused method occurs at approximately the third depth. (Fig. AO6402-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of claim 9 wherein the first energy level is higher than the second energy level.	In the accused method, the first energy level is higher than the second energy level. (Fig. AO6402-5 (Secondary Ion Mass

CLAIM	AO6402 POWER MOSFET
	Spectroscopy data).)
12. The method of claim 11 wherein the first dosage is higher than the second dosage.	In the accused method, the first dosage is higher than the second dosage. (Fig. AO6402-5 (Secondary Ion Mass Spectroscopy data).)
13. The method of claim 1 wherein the step of forming the heavy body comprises a process of diffusing dopants of the second conductivity type.	The step of the accused method in which the P-type heavy body is created includes a process in which P-type dopants (a second conductivity type) are diffused into the P-doped well. (Fig. AO6402-3 (Scanning Electron Microscopy image), item E; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item E.)
21. A method of manufacturing a trench field effect transistor on a semiconductor substrate having dopants of a first conductivity type, the method comprising:	The accused method includes making a trench field effect transistor on a silicon semiconductor substrate created with N-type dopants (a first conductivity type). (Fig. AO6402-3 (Scanning Electron Microscopy image), item A; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item A.)
etching a plurality of trenches into the semiconductor substrate to a first depth;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO6402-3 (Scanning Electron Microscopy image), item B; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item B.)
lining the plurality of trenches with dielectric layer;	The accused method includes lining each trench with a dielectric layer. (Fig. AO6402-3 (Scanning Electron Microscopy image), item G; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling the dielectric-lined plurality of trenches with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AO6402-3 (Scanning Electron Microscopy image), item B; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item B.)
forming a well between adjacent trenches to a second depth that is shallower than the first depth, the well having dopants of second conductivity type opposite to the first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate between adjacent trenches that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AO6402-3 (Scanning Electron Microscopy image), item D; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body inside the well to a third depth that is shallower than the second depth, the heavy body having dopants of the second conductivity type;	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AO6402-3 (Scanning Electron Microscopy image), item E; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item E.)

CLAIM	AO6402 POWER MOSFET
and forming a source region inside the well and adjacent to trenches, the source region having dopants of the first conductivity type, wherein, the step of forming a heavy body employs a process to form an abrupt junction between the heavy body and the well at approximately the third depth.	The accused method includes creating an N-type doped source region (a first conductivity type) inside the well and adjacent to trenches. (Fig. AO6402-3 (Scanning Electron Microscopy image), item C; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item C.) The accused method creates a change in the concentrations between the heavy body and the doped well, which forms an abrupt junction between the heavy body and the doped well at approximately the depth of the heavy body (a third depth). (Fig. AO6402-5 (Secondary Ion Mass Spectroscopy data).)
22. The method of claim 21 further comprising adjusting a location of the abrupt junction relative to the depth of the well so that a transistor breakdown current is spaced away from the trench in the semiconductor.	The depth of the abrupt junction created by the accused method is positioned relative to the depth of the well such that the peak electric field causes transistor breakdown current to be spaced away from the trench. (Fig. AO6402-3 (Scanning Electron Microscopy image), item E; Fig. AO6402-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO6402-5 (Secondary Ion Mass Spectroscopy data).)

EXHIBIT 33

EXHIBIT 33

INFRINGEMENT OF U.S. PATENT NO. 6,828,195

AOS AOL1412 POWER MOSFET

CLAIM	AOL1412 POWER MOSFET
1. A method of manufacturing a trench transistor comprising:	The AOS AOL1412 Power MOSFET is a trenched field effect transistor. (Fig. AOL1412-1 (datasheet); Fig. AOL1412-2 (package marking).) The method used to manufacture the AOL1412 power MOSFET is, by definition, a method of manufacturing a trench transistor ("the accused method").
providing a semiconductor substrate having dopants of a first conductivity type;	The accused method includes the use of a silicon semiconductor substrate with N-type dopants. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AOL1412-1 (datasheet); Fig. AOL1412-3 (Scanning Electron Microscopy image), item A; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches extending to a first depth into the semiconductor substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AOL1412-3 (Scanning Electron Microscopy image), item B; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item B.)
lining each of the plurality of trenches with a gate dielectric material;	The accused method includes lining each trench with a dielectric layer. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item G; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling each dielectric-lined trench with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item B; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item B.)
forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AOL1412-3 (Scanning Electron Microscopy image), item D; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body extending inside the doped well to a third depth that is less than said second depth of said doped well, the heavy body having dopants of the second conductivity type and forming an abrupt junction with the	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AOL1412-3 (Scanning Electron

CLAIM	AOL1412 POWER MOSFET
well;	Microscopy image), item E; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item E.) The change in concentration between the heavy body and the doped well forms an abrupt junction. (Fig. AOL1412-5 (Secondary Ion Mass Spectroscopy data).)
and forming a source region inside the well, the source region having dopants of the first conductivity types.	The accused method includes creating a source region inside the well, adjacent to the trench, having N-type dopants (a first conductivity type). (Fig. AOL1412-3 (Scanning Electron Microscopy image), item C; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item C.)
2. The method of claim 1 wherein the step of forming a doped well forms the well with a substantially flat bottom.	The doped well created by the accused method has a substantially flat bottom. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item D; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item D.)
6. The method of claim 1 wherein the step of substantially filling each dielectric-lined trench leaves a recess at an upper portion of each trench.	The step of the accused method in which the dielectric-lined trench is substantially filled with conductive polysilicon includes leaving a recess at the upper portion of each trench. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item B; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item B.)
7. The method of claim 6 further comprising filling the recess at the upper portion of each trench with dielectric material.	The accused method includes filling the recess at the upper portion of the trench with dielectric material. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item B; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item B.)
8. The method of claim 1 wherein the step of forming the heavy body comprises a double implant process.	The step of the accused method in which the P-doped heavy body is created in the P-doped well includes two implants of P-type dopants (a double implant process). (Fig. AOL1412-5 (Secondary Ion Mass Spectroscopy data).)
9. The method of claim 8 wherein the double implant process comprises:	
a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body;	The accused method includes a first implant of dopants of the second conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body. (Fig. AOL1412-5 (Secondary Ion Mass Spectroscopy data).)
and a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.	The accused method includes a second implant of dopants of the second conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body. (Fig. AOL1412-5 (Secondary Ion Mass Spectroscopy data).)
10. The method of claim 9 wherein the first implant occurs at approximately the third depth.	The first implant of the accused method occurs at approximately the third depth. (Fig. AOL1412-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of claim 9 wherein the first energy level	In the accused method, the first energy level is higher than the

CLAIM	AOL1412 POWER MOSFET
is higher than the second energy level.	second energy level. (Fig. AOL1412-5 (Secondary Ion Mass Spectroscopy data).)
12. The method of claim 11 wherein the first dosage is higher than the second dosage.	In the accused method, the first dosage is higher than the second dosage. (Fig. AOL1412-5 (Secondary Ion Mass Spectroscopy data).)
13. The method of claim 1 wherein the step of forming the heavy body comprises a process of diffusing dopants of the second conductivity type.	The step of the accused method in which the P-type heavy body is created includes a process in which P-type dopants (a second conductivity type) are diffused into the P-doped well. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item E; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item E.)
21. A method of manufacturing a trench field effect transistor on a semiconductor substrate having dopants of a first conductivity type, the method comprising:	The accused method includes making a trench field effect transistor on a silicon semiconductor substrate created with N-type dopants (a first conductivity type). (Fig. AOL1412-3 (Scanning Electron Microscopy image), item A; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item A.)
etching a plurality of trenches into the semiconductor substrate to a first depth;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AOL1412-3 (Scanning Electron Microscopy image), item B; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item B.)
lining the plurality of trenches with dielectric layer;	The accused method includes lining each trench with a dielectric layer. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item G; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling the dielectric-lined plurality of trenches with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item B; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item B.)
forming a well between adjacent trenches to a second depth that is shallower than the first depth, the well having dopants of second conductivity type opposite to the first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate between adjacent trenches that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AOL1412-3 (Scanning Electron Microscopy image), item D; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body inside the well to a third depth that is shallower than the second depth, the heavy body having dopants of the second conductivity type;	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AOL1412-3 (Scanning Electron Microscopy image), item E; Fig. AOL1412-4 (Scanning

CLAIM	AOL1412 POWER MOSFET
	Capacitance Microscopy image), item E.)
and forming a source region inside the well and adjacent to trenches, the source region having dopants of the first conductivity type, wherein, the step of forming a heavy body employs a process to form an abrupt junction between the heavy body and the well at approximately the third depth.	The accused method includes creating an N-type doped source region (a first conductivity type) inside the well and adjacent to trenches. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item C; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item C.) The accused method creates a change in the concentrations between the heavy body and the doped well, which forms an abrupt junction between the heavy body and the doped well at approximately the depth of the heavy body (a third depth). (Fig. AOL1412-5 (Secondary Ion Mass Spectroscopy data).)
22. The method of claim 21 further comprising adjusting a location of the abrupt junction relative to the depth of the well so that a transistor breakdown current is spaced away from the trench in the semiconductor.	The depth of the abrupt junction created by the accused method is positioned relative to the depth of the well such that the peak electric field causes transistor breakdown current to be spaced away from the trench. (Fig. AOL1412-3 (Scanning Electron Microscopy image), item E; Fig. AOL1412-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOL1412-5 (Secondary Ion Mass Spectroscopy data).)

EXHIBIT 34

EXHIBIT 34

INFRINGEMENT OF U.S. PATENT NO. 6,828,195

AOS AO4410 POWER MOSFET

CLAIM	AO4410 POWER MOSFET
1. A method of manufacturing a trench transistor comprising:	The AOS AO4410 Power MOSFET is a trenched field effect transistor. (Fig. AO4410-1 (datasheet); Fig. AO4410-2 (package marking).) The method used to manufacture the AO4410 power MOSFET is, by definition, a method of manufacturing a trench transistor ("the accused method").
providing a semiconductor substrate having dopants of a first conductivity type;	The accused method includes the use of a silicon semiconductor substrate with N-type dopants. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4410-1 (datasheet); Fig. AO4410-3 (Scanning Electron Microscopy image), item A; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches extending to a first depth into the semiconductor substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO4410-3 (Scanning Electron Microscopy image), item B; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item B.)
lining each of the plurality of trenches with a gate dielectric material;	The accused method includes lining each trench with a dielectric layer. (Fig. AO4410-3 (Scanning Electron Microscopy image), item G; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling each dielectric-lined trench with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AO4410-3 (Scanning Electron Microscopy image), item B; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item B.)
forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AO4410-3 (Scanning Electron Microscopy image), item D; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body extending inside the doped well to a third depth that is less than said second depth of said doped well, the heavy body having dopants of the second conductivity type and forming an abrupt junction with the	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AO4410-3 (Scanning Electron

CLAIM	AO4410 POWER MOSFET
well;	Microscopy image), item E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item E.) The change in concentration between the heavy body and the doped well forms an abrupt junction. (Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).)
and forming a source region inside the well, the source region having dopants of the first conductivity types.	The accused method includes creating a source region inside the well, adjacent to the trench, having N-type dopants (a first conductivity type). (Fig. AO4410-3 (Scanning Electron Microscopy image), item C; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item C.)
2. The method of claim 1 wherein the step of forming a doped well forms the well with a substantially flat bottom.	The doped well created by the accused method has a substantially flat bottom. (Fig. AO4410-3 (Scanning Electron Microscopy image), item D; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item D.)
6. The method of claim 1 wherein the step of substantially filling each dielectric-lined trench leaves a recess at an upper portion of each trench.	The step of the accused method in which the dielectric-lined trench is substantially filled with conductive polysilicon includes leaving a recess at the upper portion of each trench. (Fig. AO4410-3 (Scanning Electron Microscopy image), item B; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item B.)
7. The method of claim 6 further comprising filling the recess at the upper portion of each trench with dielectric material.	The accused method includes filling the recess at the upper portion of the trench with dielectric material. (Fig. AO4410-3 (Scanning Electron Microscopy image), item B; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item B.)
8. The method of claim 1 wherein the step of forming the heavy body comprises a double implant process.	The step of the accused method in which the P-doped heavy body is created in the P-doped well includes two implants of P-type dopants (a double implant process). (Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).)
9. The method of claim 8 wherein the double implant process comprises:	
a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body;	The accused method includes a first implant of dopants of the second conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body. (Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).)
and a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.	The accused method includes a second implant of dopants of the second conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body. (Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).)
10. The method of claim 9 wherein the first implant occurs at approximately the third depth.	The first implant of the accused method occurs at approximately the third depth. (Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of claim 9 wherein the first energy level is higher than the second energy level.	In the accused method, the first energy level is higher than the second energy level. (Fig. AO4410-5 (Secondary Ion Mass

CLAIM	AO4410 POWER MOSFET
	Spectroscopy data).)
12. The method of claim 11 wherein the first dosage is higher than the second dosage.	In the accused method, the first dosage is higher than the second dosage. (Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).)
13. The method of claim 1 wherein the step of forming the heavy body comprises a process of diffusing dopants of the second conductivity type.	The step of the accused method in which the P-type heavy body is created includes a process in which P-type dopants (a second conductivity type) are diffused into the P-doped well. (Fig. AO4410-3 (Scanning Electron Microscopy image), item E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item E.)
21. A method of manufacturing a trench field effect transistor on a semiconductor substrate having dopants of a first conductivity type, the method comprising:	The accused method includes making a trench field effect transistor on a silicon semiconductor substrate created with N-type dopants (a first conductivity type). (Fig. AO4410-3 (Scanning Electron Microscopy image), item A; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item A.)
etching a plurality of trenches into the semiconductor substrate to a first depth;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO4410-3 (Scanning Electron Microscopy image), item B; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item B.)
lining the plurality of trenches with dielectric layer;	The accused method includes lining each trench with a dielectric layer. (Fig. AO4410-3 (Scanning Electron Microscopy image), item G; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling the dielectric-lined plurality of trenches with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AO4410-3 (Scanning Electron Microscopy image), item B; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item B.)
forming a well between adjacent trenches to a second depth that is shallower than the first depth, the well having dopants of second conductivity type opposite to the first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate between adjacent trenches that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AO4410-3 (Scanning Electron Microscopy image), item D; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body inside the well to a third depth that is shallower than the second depth, the heavy body having dopants of the second conductivity type;	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AO4410-3 (Scanning Electron Microscopy image), item E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item E.)

CLAIM	AO4410 POWER MOSFET
and forming a source region inside the well and adjacent to trenches, the source region having dopants of the first conductivity type, wherein, the step of forming a heavy body employs a process to form an abrupt junction between the heavy body and the well at approximately the third depth.	The accused method includes creating an N-type doped source region (a first conductivity type) inside the well and adjacent to trenches. (Fig. AO4410-3 (Scanning Electron Microscopy image), item C; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item C.) The accused method creates a change in the concentrations between the heavy body and the doped well, which forms an abrupt junction between the heavy body and the doped well at approximately the depth of the heavy body (a third depth). (Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).)
22. The method of claim 21 further comprising adjusting a location of the abrupt junction relative to the depth of the well so that a transistor breakdown current is spaced away from the trench in the semiconductor.	The depth of the abrupt junction created by the accused method is positioned relative to the depth of the well such that the peak electric field causes transistor breakdown current to be spaced away from the trench. (Fig. AO4410-3 (Scanning Electron Microscopy image), item E; Fig. AO4410-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4410-5 (Secondary Ion Mass Spectroscopy data).)

EXHIBIT 35

EXHIBIT 35

INFRINGEMENT OF U.S. PATENT NO. 6,828,195

AOS AO4914 POWER MOSFET

CLAIM	AO4914 POWER MOSFET
1. A method of manufacturing a trench transistor comprising:	The AOS AO4914 Power MOSFET is a trenched field effect transistor. (Fig. AO4914-1 (datasheet); Fig. AO4914-2 (package marking).) The method used to manufacture the AO4914 power MOSFET is, by definition, a method of manufacturing a trench transistor ("the accused method").
providing a semiconductor substrate having dopants of a first conductivity type;	The accused method includes the use of a silicon semiconductor substrate with N-type dopants. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4914-1 (datasheet); Fig. AO4914-3 (Scanning Electron Microscopy image), item A; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches extending to a first depth into the semiconductor substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO4914-3 (Scanning Electron Microscopy image), item B; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item B.)
lining each of the plurality of trenches with a gate dielectric material;	The accused method includes lining each trench with a dielectric layer. (Fig. AO4914-3 (Scanning Electron Microscopy image), item G; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling each dielectric-lined trench with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AO4914-3 (Scanning Electron Microscopy image), item B; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item B.)
forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AO4914-3 (Scanning Electron Microscopy image), item D; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body extending inside the doped well to a third depth that is less than said second depth of said doped well, the heavy body having dopants of the second conductivity type and forming an abrupt junction with the	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AO4914-3 (Scanning Electron

CLAIM	AO4914 POWER MOSFET
well;	Microscopy image), item E; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item E.) The change in concentration between the heavy body and the doped well forms an abrupt junction. (Fig. AO4914-5 (Secondary Ion Mass Spectroscopy data).)
and forming a source region inside the well, the source region having dopants of the first conductivity types.	The accused method includes creating a source region inside the well, adjacent to the trench, having N-type dopants (a first conductivity type). (Fig. AO4914-3 (Scanning Electron Microscopy image), item C; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item C.)
2. The method of claim 1 wherein the step of forming a doped well forms the well with a substantially flat bottom.	The doped well created by the accused method has a substantially flat bottom. (Fig. AO4914-3 (Scanning Electron Microscopy image), item D; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item D.)
6. The method of claim 1 wherein the step of substantially filling each dielectric-lined trench leaves a recess at an upper portion of each trench.	The step of the accused method in which the dielectric-lined trench is substantially filled with conductive polysilicon includes leaving a recess at the upper portion of each trench. (Fig. AO4914-3 (Scanning Electron Microscopy image), item B; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item B.)
7. The method of claim 6 further comprising filling the recess at the upper portion of each trench with dielectric material.	The accused method includes filling the recess at the upper portion of the trench with dielectric material. (Fig. AO4914-3 (Scanning Electron Microscopy image), item B; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item B.)
8. The method of claim 1 wherein the step of forming the heavy body comprises a double implant process.	The step of the accused method in which the P-doped heavy body is created in the P-doped well includes two implants of P-type dopants (a double implant process). (Fig. AO4914-5 (Secondary Ion Mass Spectroscopy data).)
9. The method of claim 8 wherein the double implant process comprises:	
a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body;	The accused method includes a first implant of dopants of the second conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body. (Fig. AO4914-5 (Secondary Ion Mass Spectroscopy data).)
and a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.	The accused method includes a second implant of dopants of the second conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body. (Fig. AO4914-5 (Secondary Ion Mass Spectroscopy data).)
10. The method of claim 9 wherein the first implant occurs at approximately the third depth.	The first implant of the accused method occurs at approximately the third depth. (Fig. AO4914-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of claim 9 wherein the first energy level is higher than the second energy level.	In the accused method, the first energy level is higher than the second energy level. (Fig. AO4914-5 (Secondary Ion Mass

CLAIM	AO4914 POWER MOSFET
	Spectroscopy data).)
12. The method of claim 11 wherein the first dosage is higher than the second dosage.	In the accused method, the first dosage is higher than the second dosage. (Fig. AO4914-5 (Secondary Ion Mass Spectroscopy data).)
13. The method of claim 1 wherein the step of forming the heavy body comprises a process of diffusing dopants of the second conductivity type.	The step of the accused method in which the P-type heavy body is created includes a process in which P-type dopants (a second conductivity type) are diffused into the P-doped well. (Fig. AO4914-3 (Scanning Electron Microscopy image), item E; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item E.)
21. A method of manufacturing a trench field effect transistor on a semiconductor substrate having dopants of a first conductivity type, the method comprising:	The accused method includes making a trench field effect transistor on a silicon semiconductor substrate created with N-type dopants (a first conductivity type). (Fig. AO4914-3 (Scanning Electron Microscopy image), item A; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item A.)
etching a plurality of trenches into the semiconductor substrate to a first depth;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO4914-3 (Scanning Electron Microscopy image), item B; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item B.)
lining the plurality of trenches with dielectric layer;	The accused method includes lining each trench with a dielectric layer. (Fig. AO4914-3 (Scanning Electron Microscopy image), item G; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling the dielectric-lined plurality of trenches with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AO4914-3 (Scanning Electron Microscopy image), item B; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item B.)
forming a well between adjacent trenches to a second depth that is shallower than the first depth, the well having dopants of second conductivity type opposite to the first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate between adjacent trenches that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AO4914-3 (Scanning Electron Microscopy image), item D; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body inside the well to a third depth that is shallower than the second depth, the heavy body having dopants of the second conductivity type;	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AO4914-3 (Scanning Electron Microscopy image), item E; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item E.)

CLAIM	AO4914 POWER MOSFET
and forming a source region inside the well and adjacent to trenches, the source region having dopants of the first conductivity type, wherein, the step of forming a heavy body employs a process to form an abrupt junction between the heavy body and the well at approximately the third depth.	The accused method includes creating an N-type doped source region (a first conductivity type) inside the well and adjacent to trenches. (Fig. AO4914-3 (Scanning Electron Microscopy image), item C; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item C.) The accused method creates a change in the concentrations between the heavy body and the doped well, which forms an abrupt junction between the heavy body and the doped well at approximately the depth of the heavy body (a third depth). (Fig. AO4914-5 (Secondary Ion Mass Spectroscopy data).)
22. The method of claim 21 further comprising adjusting a location of the abrupt junction relative to the depth of the well so that a transistor breakdown current is spaced away from the trench in the semiconductor.	The depth of the abrupt junction created by the accused method is positioned relative to the depth of the well such that the peak electric field causes transistor breakdown current to be spaced away from the trench. (Fig. AO4914-3 (Scanning Electron Microscopy image), item E; Fig. AO4914-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4914-5 (Secondary Ion Mass Spectroscopy data).)

EXHIBIT 36

EXHIBIT 36

INFRINGEMENT OF U.S. PATENT NO. 6,828,195

AOS AO4422 POWER MOSFET

CLAIM	AO4422 POWER MOSFET
1. A method of manufacturing a trench transistor comprising:	The AOS AO4422 Power MOSFET is a trenched field effect transistor. (Fig. AO4422-1 (datasheet); Fig. AO4422-2 (package marking).) The method used to manufacture the AO4422 power MOSFET is, by definition, a method of manufacturing a trench transistor ("the accused method").
providing a semiconductor substrate having dopants of a first conductivity type;	The accused method includes the use of a silicon semiconductor substrate with N-type dopants. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4422-1 (datasheet); Fig. AO4422-3 (Scanning Electron Microscopy image), item A; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches extending to a first depth into the semiconductor substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO4422-3 (Scanning Electron Microscopy image), item B; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item B.)
lining each of the plurality of trenches with a gate dielectric material;	The accused method includes lining each trench with a dielectric layer. (Fig. AO4422-3 (Scanning Electron Microscopy image), item G; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling each dielectric-lined trench with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AO4422-3 (Scanning Electron Microscopy image), item B; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item B.)
forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AO4422-3 (Scanning Electron Microscopy image), item D; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body extending inside the doped well to a third depth that is less than said second depth of said doped well, the heavy body having dopants of the second conductivity type and forming an abrupt junction with the	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AO4422-3 (Scanning Electron

CLAIM	AO4422 POWER MOSFET
well;	Microscopy image), item E; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item E.) The change in concentration between the heavy body and the doped well forms an abrupt junction. (Fig. AO4422-5 (Secondary Ion Mass Spectroscopy data).)
and forming a source region inside the well, the source region having dopants of the first conductivity types.	The accused method includes creating a source region inside the well, adjacent to the trench, having N-type dopants (a first conductivity type). (Fig. AO4422-3 (Scanning Electron Microscopy image), item C; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item C.)
2. The method of claim 1 wherein the step of forming a doped well forms the well with a substantially flat bottom.	The doped well created by the accused method has a substantially flat bottom. (Fig. AO4422-3 (Scanning Electron Microscopy image), item D; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item D.)
6. The method of claim 1 wherein the step of substantially filling each dielectric-lined trench leaves a recess at an upper portion of each trench.	The step of the accused method in which the dielectric-lined trench is substantially filled with conductive polysilicon includes leaving a recess at the upper portion of each trench. (Fig. AO4422-3 (Scanning Electron Microscopy image), item B; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item B.)
7. The method of claim 6 further comprising filling the recess at the upper portion of each trench with dielectric material.	The accused method includes filling the recess at the upper portion of the trench with dielectric material. (Fig. AO4422-3 (Scanning Electron Microscopy image), item B; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item B.)
8. The method of claim 1 wherein the step of forming the heavy body comprises a double implant process.	The step of the accused method in which the P-doped heavy body is created in the P-doped well includes two implants of P-type dopants (a double implant process). (Fig. AO4422-5 (Secondary Ion Mass Spectroscopy data).)
9. The method of claim 8 wherein the double implant process comprises:	
a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body;	The accused method includes a first implant of dopants of the second conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body. (Fig. AO4422-5 (Secondary Ion Mass Spectroscopy data).)
and a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.	The accused method includes a second implant of dopants of the second conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body. (Fig. AO4422-5 (Secondary Ion Mass Spectroscopy data).)
10. The method of claim 9 wherein the first implant occurs at approximately the third depth.	The first implant of the accused method occurs at approximately the third depth. (Fig. AO4422-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of claim 9 wherein the first energy level is higher than the second energy level.	In the accused method, the first energy level is higher than the second energy level. (Fig. AO4422-5 (Secondary Ion Mass

CLAIM	AO4422 POWER MOSFET
	Spectroscopy data).)
12. The method of claim 11 wherein the first dosage is higher than the second dosage.	In the accused method, the first dosage is higher than the second dosage. (Fig. AO4422-5 (Secondary Ion Mass Spectroscopy data).)
13. The method of claim 1 wherein the step of forming the heavy body comprises a process of diffusing dopants of the second conductivity type.	The step of the accused method in which the P-type heavy body is created includes a process in which P-type dopants (a second conductivity type) are diffused into the P-doped well. (Fig. AO4422-3 (Scanning Electron Microscopy image), item E; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item E.)
21. A method of manufacturing a trench field effect transistor on a semiconductor substrate having dopants of a first conductivity type, the method comprising:	The accused method includes making a trench field effect transistor on a silicon semiconductor substrate created with N-type dopants (a first conductivity type). (Fig. AO4422-3 (Scanning Electron Microscopy image), item A; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item A.)
etching a plurality of trenches into the semiconductor substrate to a first depth;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO4422-3 (Scanning Electron Microscopy image), item B; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item B.)
lining the plurality of trenches with dielectric layer;	The accused method includes lining each trench with a dielectric layer. (Fig. AO4422-3 (Scanning Electron Microscopy image), item G; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling the dielectric-lined plurality of trenches with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AO4422-3 (Scanning Electron Microscopy image), item B; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item B.)
forming a well between adjacent trenches to a second depth that is shallower than the first depth, the well having dopants of second conductivity type opposite to the first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate between adjacent trenches that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AO4422-3 (Scanning Electron Microscopy image), item D; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body inside the well to a third depth that is shallower than the second depth, the heavy body having dopants of the second conductivity type;	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AO4422-3 (Scanning Electron Microscopy image), item E; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item E.)

CLAIM	AO4422 POWER MOSFET
and forming a source region inside the well and adjacent to trenches, the source region having dopants of the first conductivity type, wherein, the step of forming a heavy body employs a process to form an abrupt junction between the heavy body and the well at approximately the third depth.	The accused method includes creating an N-type doped source region (a first conductivity type) inside the well and adjacent to trenches. (Fig. AO4422-3 (Scanning Electron Microscopy image), item C; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item C.) The accused method creates a change in the concentrations between the heavy body and the doped well, which forms an abrupt junction between the heavy body and the doped well at approximately the depth of the heavy body (a third depth). (Fig. AO4422-5 (Secondary Ion Mass Spectroscopy data).)
22. The method of claim 21 further comprising adjusting a location of the abrupt junction relative to the depth of the well so that a transistor breakdown current is spaced away from the trench in the semiconductor.	The depth of the abrupt junction created by the accused method is positioned relative to the depth of the well such that the peak electric field causes transistor breakdown current to be spaced away from the trench. (Fig. AO4422-3 (Scanning Electron Microscopy image), item E; Fig. AO4422-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4422-5 (Secondary Ion Mass Spectroscopy data).)

EXHIBIT 37

EXHIBIT 37

INFRINGEMENT OF U.S. PATENT NO. 6,828,195

AOS AO4704 POWER MOSFET

CLAIM	AO4704 POWER MOSFET
1. A method of manufacturing a trench transistor comprising:	The AOS AO4704 Power MOSFET is a trenched field effect transistor. (Fig. AO4704-1 (datasheet); Fig. AO4704-2 (package marking).) The method used to manufacture the AO4704 power MOSFET is, by definition, a method of manufacturing a trench transistor ("the accused method").
providing a semiconductor substrate having dopants of a first conductivity type;	The accused method includes the use of a silicon semiconductor substrate with N-type dopants. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AO4704-1 (datasheet); Fig. AO4704-3 (Scanning Electron Microscopy image), item A; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches extending to a first depth into the semiconductor substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO4704-3 (Scanning Electron Microscopy image), item B; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item B.)
lining each of the plurality of trenches with a gate dielectric material;	The accused method includes lining each trench with a dielectric layer. (Fig. AO4704-3 (Scanning Electron Microscopy image), item G; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling each dielectric-lined trench with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AO4704-3 (Scanning Electron Microscopy image), item B; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item B.)
forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AO4704-3 (Scanning Electron Microscopy image), item D; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body extending inside the doped well to a third depth that is less than said second depth of said doped well, the heavy body having dopants of the second conductivity type and forming an abrupt junction with the	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AO4704-3 (Scanning Electron

CLAIM	AO4704 POWER MOSFET
well;	Microscopy image), item E; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item E.) The change in concentration between the heavy body and the doped well forms an abrupt junction. (Fig. AO4704-5 (Secondary Ion Mass Spectroscopy data).)
and forming a source region inside the well, the source region having dopants of the first conductivity types.	The accused method includes creating a source region inside the well, adjacent to the trench, having N-type dopants (a first conductivity type). (Fig. AO4704-3 (Scanning Electron Microscopy image), item C; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item C.)
2. The method of claim 1 wherein the step of forming a doped well forms the well with a substantially flat bottom.	The doped well created by the accused method has a substantially flat bottom. (Fig. AO4704-3 (Scanning Electron Microscopy image), item D; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item D.)
6. The method of claim 1 wherein the step of substantially filling each dielectric-lined trench leaves a recess at an upper portion of each trench.	The step of the accused method in which the dielectric-lined trench is substantially filled with conductive polysilicon includes leaving a recess at the upper portion of each trench. (Fig. AO4704-3 (Scanning Electron Microscopy image), item B; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item B.)
7. The method of claim 6 further comprising filling the recess at the upper portion of each trench with dielectric material.	The accused method includes filling the recess at the upper portion of the trench with dielectric material. (Fig. AO4704-3 (Scanning Electron Microscopy image), item B; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item B.)
8. The method of claim 1 wherein the step of forming the heavy body comprises a double implant process.	The step of the accused method in which the P-doped heavy body is created in the P-doped well includes two implants of P-type dopants (a double implant process). (Fig. AO4704-5 (Secondary Ion Mass Spectroscopy data).)
9. The method of claim 8 wherein the double implant process comprises:	
a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body;	The accused method includes a first implant of dopants of the second conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body. (Fig. AO4704-5 (Secondary Ion Mass Spectroscopy data).)
and a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.	The accused method includes a second implant of dopants of the second conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body. (Fig. AO4704-5 (Secondary Ion Mass Spectroscopy data).)
10. The method of claim 9 wherein the first implant occurs at approximately the third depth.	The first implant of the accused method occurs at approximately the third depth. (Fig. AO4704-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of claim 9 wherein the first energy level is higher than the second energy level.	In the accused method, the first energy level is higher than the second energy level. (Fig. AO4704-5 (Secondary Ion Mass

CLAIM	AO4704 POWER MOSFET
	Spectroscopy data).)
12. The method of claim 11 wherein the first dosage is higher than the second dosage.	In the accused method, the first dosage is higher than the second dosage. (Fig. AO4704-5 (Secondary Ion Mass Spectroscopy data).)
13. The method of claim 1 wherein the step of forming the heavy body comprises a process of diffusing dopants of the second conductivity type.	The step of the accused method in which the P-type heavy body is created includes a process in which P-type dopants (a second conductivity type) are diffused into the P-doped well. (Fig. AO4704-3 (Scanning Electron Microscopy image), item E; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item E.)
21. A method of manufacturing a trench field effect transistor on a semiconductor substrate having dopants of a first conductivity type, the method comprising:	The accused method includes making a trench field effect transistor on a silicon semiconductor substrate created with N-type dopants (a first conductivity type). (Fig. AO4704-3 (Scanning Electron Microscopy image), item A; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item A.)
etching a plurality of trenches into the semiconductor substrate to a first depth;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO4704-3 (Scanning Electron Microscopy image), item B; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item B.)
lining the plurality of trenches with dielectric layer;	The accused method includes lining each trench with a dielectric layer. (Fig. AO4704-3 (Scanning Electron Microscopy image), item G; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling the dielectric-lined plurality of trenches with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AO4704-3 (Scanning Electron Microscopy image), item B; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item B.)
forming a well between adjacent trenches to a second depth that is shallower than the first depth, the well having dopants of second conductivity type opposite to the first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate between adjacent trenches that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AO4704-3 (Scanning Electron Microscopy image), item D; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body inside the well to a third depth that is shallower than the second depth, the heavy body having dopants of the second conductivity type;	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AO4704-3 (Scanning Electron Microscopy image), item E; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item E.)

CLAIM	AO4704 POWER MOSFET
and forming a source region inside the well and adjacent to trenches, the source region having dopants of the first conductivity type, wherein, the step of forming a heavy body employs a process to form an abrupt junction between the heavy body and the well at approximately the third depth.	The accused method includes creating an N-type doped source region (a first conductivity type) inside the well and adjacent to trenches. (Fig. AO4704-3 (Scanning Electron Microscopy image), item C; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item C.) The accused method creates a change in the concentrations between the heavy body and the doped well, which forms an abrupt junction between the heavy body and the doped well at approximately the depth of the heavy body (a third depth). (Fig. AO4704-5 (Secondary Ion Mass Spectroscopy data).)
22. The method of claim 21 further comprising adjusting a location of the abrupt junction relative to the depth of the well so that a transistor breakdown current is spaced away from the trench in the semiconductor.	The depth of the abrupt junction created by the accused method is positioned relative to the depth of the well such that the peak electric field causes transistor breakdown current to be spaced away from the trench. (Fig. AO4704-3 (Scanning Electron Microscopy image), item E; Fig. AO4704-4 (Scanning Capacitance Microscopy image), item E.; Fig. AO4704-5 (Secondary Ion Mass Spectroscopy data).)

EXHIBIT 38

EXHIBIT 38

INFRINGEMENT OF U.S. PATENT NO. 6,828,195

AOS AOD414 POWER MOSFET

CLAIM	AOD414 POWER MOSFET
1. A method of manufacturing a trench transistor comprising:	The AOS AOD414 Power MOSFET is a trenched field effect transistor. (Fig. AOD414-1 (datasheet); Fig. AOD414-2 (package marking).) The method used to manufacture the AOD414 power MOSFET is, by definition, a method of manufacturing a trench transistor ("the accused method").
providing a semiconductor substrate having dopants of a first conductivity type;	The accused method includes the use of a silicon semiconductor substrate with N-type dopants. In the language of the claim, the N-type dopants in the substrate are a "first conductivity type." (Fig. AOD414-1 (datasheet); Fig. AOD414-3 (Scanning Electron Microscopy image), item A; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item A.)
forming a plurality of trenches extending to a first depth into the semiconductor substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AOD414-3 (Scanning Electron Microscopy image), item B; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item B.)
lining each of the plurality of trenches with a gate dielectric material;	The accused method includes lining each trench with a dielectric layer. (Fig. AOD414-3 (Scanning Electron Microscopy image), item G; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling each dielectric-lined trench with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AOD414-3 (Scanning Electron Microscopy image), item B; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item B.)
forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AOD414-3 (Scanning Electron Microscopy image), item D; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body extending inside the doped well to a third depth that is less than said second depth of said doped well, the heavy body having dopants of the second conductivity type and forming an abrupt junction with the	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AOD414-3 (Scanning Electron

CLAIM	AOD414 POWER MOSFET
well;	Microscopy image), item E; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item E.) The change in concentration between the heavy body and the doped well forms an abrupt junction. (Fig. AOD414-5 (Secondary Ion Mass Spectroscopy data).)
and forming a source region inside the well, the source region having dopants of the first conductivity types.	The accused method includes creating a source region inside the well, adjacent to the trench, having N-type dopants (a first conductivity type). (Fig. AOD414-3 (Scanning Electron Microscopy image), item C; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item C.)
2. The method of claim 1 wherein the step of forming a doped well forms the well with a substantially flat bottom.	The doped well created by the accused method has a substantially flat bottom. (Fig. AOD414-3 (Scanning Electron Microscopy image), item D; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item D.)
6. The method of claim 1 wherein the step of substantially filling each dielectric-lined trench leaves a recess at an upper portion of each trench.	The step of the accused method in which the dielectric-lined trench is substantially filled with conductive polysilicon includes leaving a recess at the upper portion of each trench. (Fig. AOD414-3 (Scanning Electron Microscopy image), item B; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item B.)
7. The method of claim 6 further comprising filling the recess at the upper portion of each trench with dielectric material.	The accused method includes filling the recess at the upper portion of the trench with dielectric material. (Fig. AOD414-3 (Scanning Electron Microscopy image), item B; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item B.)
8. The method of claim 1 wherein the step of forming the heavy body comprises a double implant process.	The step of the accused method in which the P-doped heavy body is created in the P-doped well includes two implants of P-type dopants (a double implant process). (Fig. AOD414-5 (Secondary Ion Mass Spectroscopy data).)
9. The method of claim 8 wherein the double implant process comprises:	
a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body;	The accused method includes a first implant of dopants of the second conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body. (Fig. AOD414-5 (Secondary Ion Mass Spectroscopy data).)
and a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.	The accused method includes a second implant of dopants of the second conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body. (Fig. AOD414-5 (Secondary Ion Mass Spectroscopy data).)
10. The method of claim 9 wherein the first implant occurs at approximately the third depth.	The first implant of the accused method occurs at approximately the third depth. (Fig. AOD414-5 (Secondary Ion Mass Spectroscopy data).)
11. The method of claim 9 wherein the first energy level	In the accused method, the first energy level is higher than the

CLAIM	AOD414 POWER MOSFET
is higher than the second energy level.	second energy level. (Fig. AOD414-5 (Secondary Ion Mass Spectroscopy data).)
12. The method of claim 11 wherein the first dosage is higher than the second dosage.	In the accused method, the first dosage is higher than the second dosage. (Fig. AOD414-5 (Secondary Ion Mass Spectroscopy data).)
13. The method of claim 1 wherein the step of forming the heavy body comprises a process of diffusing dopants of the second conductivity type.	The step of the accused method in which the P-type heavy body is created includes a process in which P-type dopants (a second conductivity type) are diffused into the P-doped well. (Fig. AOD414-3 (Scanning Electron Microscopy image), item E; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item E.)
21. A method of manufacturing a trench field effect transistor on a semiconductor substrate having dopants of a first conductivity type, the method comprising:	The accused method includes making a trench field effect transistor on a silicon semiconductor substrate created with N-type dopants (a first conductivity type). (Fig. AOD414-3 (Scanning Electron Microscopy image), item A; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item A.)
etching a plurality of trenches into the semiconductor substrate to a first depth;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AOD414-3 (Scanning Electron Microscopy image), item B; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item B.)
lining the plurality of trenches with dielectric layer;	The accused method includes lining each trench with a dielectric layer. (Fig. AOD414-3 (Scanning Electron Microscopy image), item G; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item G.)
substantially filling the dielectric-lined plurality of trenches with conductive material;	The accused method includes substantially filling each dielectric-lined trench with doped polysilicon, a conductive material. (Fig. AOD414-3 (Scanning Electron Microscopy image), item B; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item B.)
forming a well between adjacent trenches to a second depth that is shallower than the first depth, the well having dopants of second conductivity type opposite to the first conductivity type;	The accused method includes creating a P-type (a second conductivity type opposite to the first conductivity type) doped well in the substrate between adjacent trenches that extends to a depth (a second depth) that is less than the depth of the plurality of trenches (the first depth). (Fig. AOD414-3 (Scanning Electron Microscopy image), item D; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item D.)
forming a heavy body inside the well to a third depth that is shallower than the second depth, the heavy body having dopants of the second conductivity type;	The accused method includes creating a P-type heavy body (a second conductivity type) that extends to a depth (a third depth) that is less than the depth of the P-type doped well (the second depth). (Fig. AOD414-3 (Scanning Electron Microscopy image), item E; Fig. AOD414-4 (Scanning

CLAIM	AOD414 POWER MOSFET
	Capacitance Microscopy image), item E.)
and forming a source region inside the well and adjacent to trenches, the source region having dopants of the first conductivity type, wherein, the step of forming a heavy body employs a process to form an abrupt junction between the heavy body and the well at approximately the third depth.	The accused method includes creating an N-type doped source region (a first conductivity type) inside the well and adjacent to trenches. (Fig. AOD414-3 (Scanning Electron Microscopy image), item C; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item C.) The accused method creates a change in the concentrations between the heavy body and the doped well, which forms an abrupt junction between the heavy body and the doped well at approximately the depth of the heavy body (a third depth). (Fig. AOD414-5 (Secondary Ion Mass Spectroscopy data).)
22. The method of claim 21 further comprising adjusting a location of the abrupt junction relative to the depth of the well so that a transistor breakdown current is spaced away from the trench in the semiconductor.	The depth of the abrupt junction created by the accused method is positioned relative to the depth of the well such that the peak electric field causes transistor breakdown current to be spaced away from the trench. (Fig. AOD414-3 (Scanning Electron Microscopy image), item E; Fig. AOD414-4 (Scanning Capacitance Microscopy image), item E.; Fig. AOD414-5 (Secondary Ion Mass Spectroscopy data).)